

# Uplynx XS8001-T SOC Technical Brief

ESCD-UPLYNX-007 Version 1.0

**ESMT Inc.**

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Preliminary

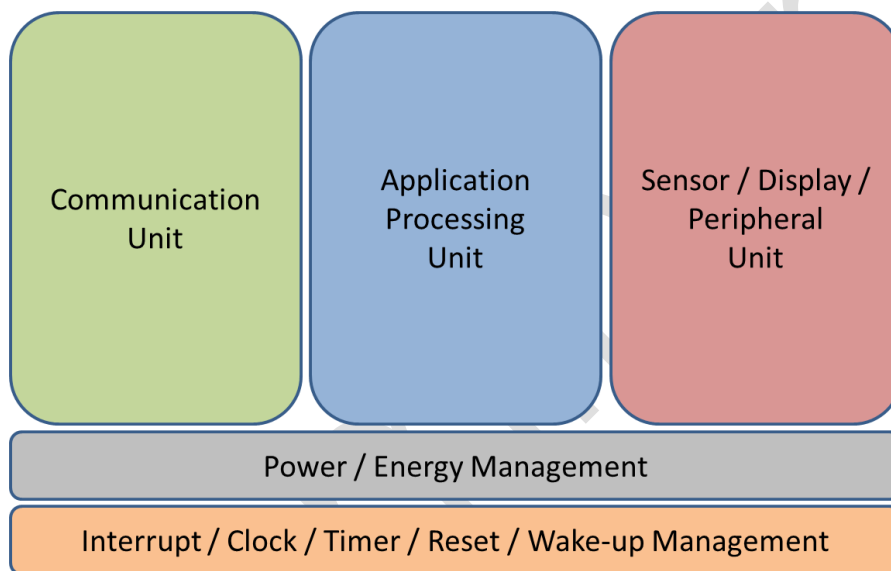
**1 Product Overview**

The Uplynx XS8001-T is one of ESMTs family of wireless SOCs designed for ultra-low-power wireless IoT applications.

The Uplynx XS8001-T monolithically integrates the Sigfox protocol stack with best-in-class sub-GHz RF performance.

The Uplynx XS8001-T’s built-in 10-bit ADC, analogue comparators and GPIOs are available for access via an AT command set over UART interface.

The Uplynx XS8001-T is the most cost effective, smallest, and easy-to-design SOC solution for IoT applications where wireless data uplink is enabled via the Sigfox network.



**Figure 1-1 Functional Blocks**

**2 Product Features**

**2.1 Communication Unit**

- 868 (863~870) MHz, 870-875.6MHz, 915 (902-928) MHz ISM band support
- State-of-the-art integrated RF front-end with high-performance synthesizer and integrated power amplifier
- Programmable PA output power up to 22dBm
- Sigfox™ uplink compliant RF signaling via tight Power Amplifier profiling and phase shaping
- Sigfox Verified™ reference circuit for RCZ1,2,3,4 (5,6) AT command set
- Build in channel power detector for LBT implementation

## 2.2 Application Processing Unit

- ANDES 32-bit AndesCore N801-S processor
- Energy-Efficient
- Programmable up to 60MHz
- Up to 128kB embedded FLASH
- 8kB Instruction RAM for time-critical tasks or data memory extension
- Up to 24kB Data RAM with retention
- Supports 10-channel Direct Memory Access (DMA)
- AES-128 ciphering and deciphering hardware engine with CCM support
- Arithmetic coding engine for data compression/decompression

## 2.3 Sensor / Display / Peripheral Unit

- GPIOs for general peripheral support
- SPI, I2C, UART,
- 2x 32-bits PWM Engines with two channels each
- 4-channel 10-bit on-chip ADC for external analog sources
- Embedded on-chip monolithic temperature sensor
- Low-power analog comparator with wake-up support
- Programmable supply detect alarm (AVDD) for battery monitoring

## 2.4 Interrupt / Clock / Timer / Reset / Wake-up Management

- Built-in power-on-reset (POR)
- On-chip low-power 32kHz oscillator
- Integrated 12MHz crystal oscillator driver, support external 24MHz TCXO
- Fine-grain dynamic PLL frequency setting for optimal power / performance
- Real-Time-Clock (RTC)
- Watch-Dog Timer (WDT)
- 3x 32-bit general-purpose fast timer
- 3x 32-bit ultra-low-power timers with wake-up support

## 2.5 Power / Energy Management

- VDD = 2.5V – 3.5V (Sigfox verified reference design at 2.5V and 3.3V for RCZ1 and RCZ2/4 respectively)
- Operating temperature -40°C to 85°C
- Multiple internal LDOs for supply noise immunity and optimized performance
- Sigfox Tx mode: Typically 58mA at 14dBm output (Tx + Sigfox AT uplink modem)
- Integrated power management engine to optimize energy consumption
  - *Normal* mode: full features with clock speed up to 60MHz
  - *Idle* mode: Normal mode with CPU clock-gated for power-saving
  - *Sleep* mode: System in hibernate except SRAM and partial digital register bank in retention for fast wake-up

2.6 Small Form-Factor

- Available in 7mm x 7mm 48-pin QFN package
- Compact board design with very low external component count

2.7 Easy-to-Design

- The Uplynx XS8001-T comes with a complete set of technical documents. They include basic product briefs, datasheets, technical reference manuals as well as many application notes.
- The Uplynx XS8001-T comes with a baseboard for development and/or evaluation.

3 Functional Block

Shown below is the functional block diagram for the 48-pin version of the Uplynx XS8001-T, which includes an EBI (external bus interface), used to implement additional memory on board, e.g. pseudo SRAM.

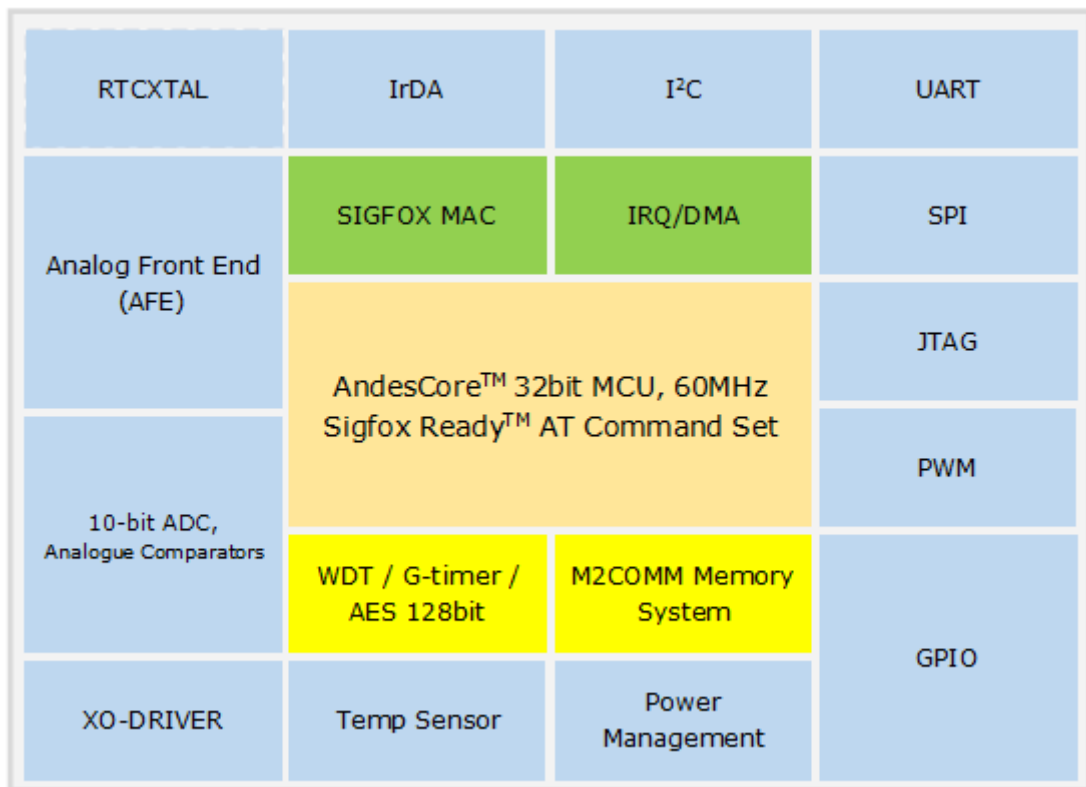


Figure 3-1 Functional Block Diagram

## 4 Pin-out and package mechanicals

### 4.1 QFN48 Pinout

Pin Number	Pin Name	Pin Type	Description
1	RF_TX_OUT	A	RF Power Amplifier Output
2	NC		Not used
3	TDSW		Not used.
4	RF_RX_N	A	LNA N- input
5	RF_RX_P	A	LNA P- input
6	VDDA	P	Analog 3.3V decoupling pin (Direct connection to main power is NOT a must)
7	ADGPIO1	A	Analog input to analog comparator channel 7 [ACMP_CH7]
		A	Analog input to MADC channel 1 [SAR_CH1] (0~2.5V)
	GPIO0	I/O	General purpose digital I/O pin [GPIO0]. See GPIO section for a complete description.
8	ADGPIO2	A	Analog input to analog comparator channel 1 [ACMP_CH1]
		A	Analog input to MADC channel 2 [SAR_CH2] (0~2.5V)
	GPIO4	I/O	General purpose digital I/O pin [GPIO4]. See GPIO section for a complete description.
9	ADGPIO3	I	Calibration use , this pin must be connected to system ground
10	ADGPIO4	A	Analog input to analog comparator channel 3 [ACMP_CH3]
		A	Analog input to MADC channel 5 [SAR_CH5] (0~1.2V)
	GPIO17	I/O	General purpose digital I/O pin [GPIO17]. See GPIO section for a complete description.
11	ADGPIO5	A	Analog input to analog comparator channel 4 [ACMP_CH4]
		A	Analog input to MADC channel 6 [SAR_CH6] (0~1.2V)
	GPIO29	I/O	General purpose digital I/O pin [GPIO29]. See GPIO section for a complete description.
12	ADGPIO6	A	Analog input to analog comparator channel 5 [ACMP_CH5]
		I/O	General purpose digital I/O pin [GPIO30]. See GPIO section for a complete description.
13	XTAL_IN	A	Crystal oscillator input
14	XTAL_OUT	A	Crystal oscillator output
15	GPIO1	I/O	General purpose digital I/O pin [GPIO1]. See GPIO section for a complete description.
	PWM0	O	PWM0 channel 0 output
16	GPIO2	I/O	General purpose digital I/O pin [GPIO2]. See GPIO section for a complete description.
	BOOTEN	I	When it is pulled low at power up, the bootloader is initiated. Refer to Uplynx Products (Addendum - Boot Procedure) (AN-UPLYNX-003).pdf for details
	PWM1	O	PWM0 channel 1 output
17	UART0_TX	O	UART0 data transmitter output pin
	GPIO19	I/O	General purpose digital I/O pin [GPIO19]. See GPIO section for a complete description.
18	UART0_RX	I	UART0 data receiver input pin
	GPIO20	I/O	General purpose digital I/O pin [GPIO20]. See GPIO section for a complete description.

Pin Number	Pin Name	Pin Type	Description
19	I2C_CLK	O	I2C clock pin
	GPIO21	I/O	General purpose digital I/O pin [GPIO21]. See GPIO section for a complete description.
	PWM2	O	PWM1 channel 0 output
20	I2C_SDA	I/O	I2C data I/O pin
	GPIO22	I/O	General purpose digital I/O pin [GPIO22]. See GPIO section for a complete description.
	PWM3	O	PWM1 channel 1 output
21	JDAT	I/O	JTAG data I/O pin
22	JCLK	I	JTAG clock pin
23	UART1_RX	I	UART1 data receiver input pin
	GPIO23	I/O	General purpose digital I/O pin [GPIO23]. See GPIO section for a complete description.
24	UART1_TX	O	UART1 data transmitter output pin
	GPIO24	I/O	General purpose digital I/O pin [GPIO24]. See GPIO section for a complete description.
25	VDDD	P	Digital power
26	VDIG	A	Core voltage
27	RTC_XTAL_OUT	A	32KHz crystal oscillator output
28	RTC_XTAL_IN	A	32KHz crystal oscillator input
29	GPIO5	I/O	General purpose digital I/O pin [GPIO5]. See GPIO section for a complete description.
	SPI1_MISO	I/O	SPI1 master in / slave out pin.
30	GPIO6	I/O	General purpose digital I/O pin [GPIO6]. See GPIO section for a complete description.
31	GPIO7	I/O	General purpose digital I/O pin [GPIO7]. See GPIO section for a complete description.
	SPI0_CS1	O	SPI0 second chip select pin
32	SYS_RSTN	I	System reset pin – Active Low
33	GPIO9	I/O	General purpose digital I/O pin [GPIO9]. See GPIO section for a complete description.
	SPI1_MOSI	I/O	SPI1 master out / slave in pin
	INT0	I	external interrupt INT0
34	SPI1_CSN	O	SPI1 chip select pin
	GPIO10	I/O	General purpose digital I/O pin [GPIO10]. See GPIO section for a complete description.
35	SPI0_MOSI	I/O	SPI0 master out / slave in pin
	GPIO25	I/O	General purpose digital I/O pin [GPIO25]. See GPIO section for a complete description.
36	SPI0_MISO	I/O	SPI0 master in / slave out pin
	GPIO26	I/O	General purpose digital I/O pin [GPIO26]. See GPIO section for a complete description.
37	SPI0_CLK	O	SPI0 clock pin
	GPIO27	I/O	General purpose digital I/O pin [GPIO27]. See GPIO section for a complete description.

Pin Number	Pin Name	Pin Type	Description
38	SPIO_CSNO	O	SPIO first chip select pin
	GPIO28	I/O	General purpose digital I/O pin [GPIO28]. See GPIO section for a complete description.
	TCXO_PD	O	Power down signal for TCXO
39	SPI1_CLK	O	SPI1 clock pin
	GPIO11	I/O	General purpose digital I/O pin [GPIO11]. See GPIO section for a complete description.
40	GPIO12	I/O	General purpose digital I/O pin [GPIO12]. See GPIO section for a complete description.
	INT1	I	External interrupt INT1
41	GPIO13	I/O	General purpose digital I/O pin [GPIO13]. See GPIO section for a complete description.
42	GPIO14	I/O	General purpose digital I/O pin [GPIO14]. See GPIO section for a complete description.
43	GPIO15	I/O	General purpose digital I/O pin [GPIO15]. See GPIO section for a complete description.
44	CAPCHGE	O	LDO pre-charge/pre-discharge
45	VADCREF		Not used
46	VDDA	P	Analog power
47	VDDTX	P	Analog power
48	VDDRF	P	Analog power

**Table 4-1 XS8001-T/XS8001-T QFN48 Pin Designations**

Pin Type	Description
O	Digital Output Pin
I	Digital Input Pin
A	Analog Pin
G	Ground Pin
P	Power Pin

**Table 4-2 Pin Type Description**

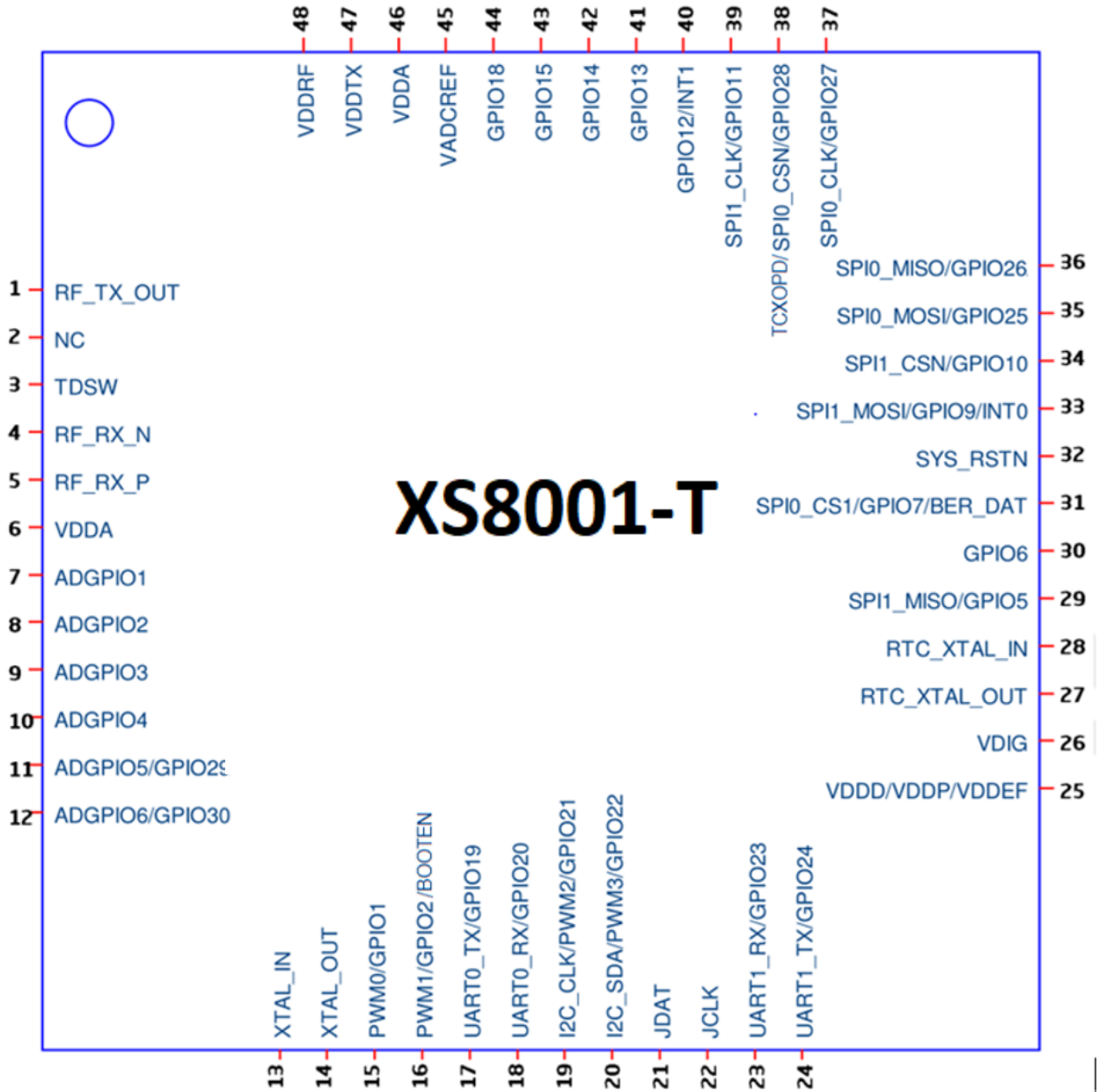


Figure 4-1 Uplynx XS8001-T and XS8001-T symbol(QFN48)

4.2 48-pin QFN Package Outline

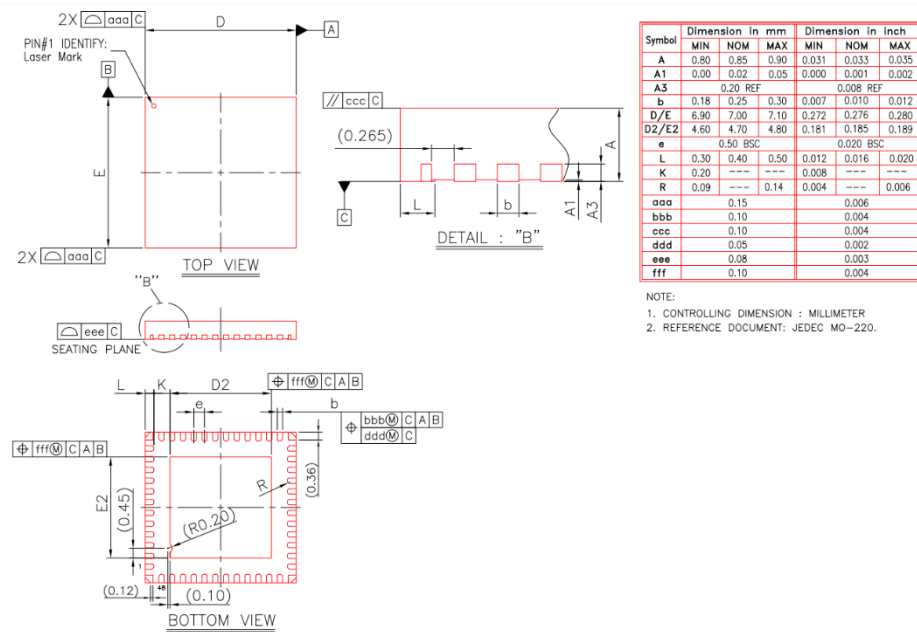


Figure 4-2 XS8001-T/XS8001-T QFN-48 Package Outline

5 Electrical Specifications

Parameter	Note	Min	Max	Unit
RF/Analogue Domain Power (VDDA, VDDRF, VDDD)		-0.3	3.5	V
Voltage on PA_OUT	DC		3.5	V
Voltage on GPIO/ADGPIO		-0.3	3.5	V
Voltage on XO12M, XI12M, XO32k and XI32k		-0.3	1.5	V
Voltage on GPIO as input		-0.3	3.5	V
Storage Temperature		-40	140	°C

Table 5-1 Absolute Maximum Ratings

Parameter	Min	Typ.	Max	Unit
RF/Analogue Domain Power (VDDA, VDDRF, VDDD)	2.5		3.5	V
Operating Temperature	-40		85	°C

Table 5-2 Recommended Operating Conditions

Parameter	Note	Min	Typ.	Max	Unit
ESD (human body model)	All pin			±2000	V
ESD (charged device model)	All pin			±500	V
ESD (machine model)	Non-RF Pin			±200	V
ESD (machine model)	RF Pin (1)			+150	V

(1) TX, XO\_IN, XO\_OUT

Table 5-3 Environmental Characteristics

Parameter	Condition/Note	Min	Typ.	Max	Unit
Output power (VDD=3.3V)	1dBm step between 7~22dBm	7		23	dBm
Power step size	from 7dBm to 22dBm	0.5	1		dB

**Table 5-4 Transmitter RF Performance**

Parameter	Min	Typ.	Max	Unit
Reference Frequency		12/24		MHz
Frequency Range	778		960	MHz

**Table 5-5 Synthesizer Specification**

Parameter	Condition/Note	Min	Typ.	Max	Unit
Input Voltage		0.1		VDD-0.1	V
Hysteresis	mode 1		±5		mV
	mode 2		±20		mV
	mode 3		±35		mV
	mode 4		±45		mV
Settling Time			135		us
Internal Reference (VDDA scalar)		2/33		30/33	VDD
Internal Reference (potential difference across an internal resistor with a fix current)		190		960	mV

**Table 5-6 Analogue Comparator ACMP0 / ACMP1 Specification**

Parameter	Condition/Note	Min	Typ.	Max	Unit
Battery Voltage tipping point	Configurable [1.6V, 1.8V, 2V and 2.5V]	1.6	1.8	2.5	V

**Table 5-7 Battery Monitor Specification**

Parameter	Condition/Note	Min	Typ.	Max	Unit
Resolution			10		Bit
AVDD Range			1.8 - 3.5		V
Full Scale	AVDD >3.0		2.5		V
Full Scale	AVDD <3.0		1.2		V
Conversion Rate				250	kHz

**Table 5-8 Monitoring ADC Specification**

## 6 Preloaded Software

The Uplynx products are loaded with the following software prior shipping:

Product	Bootloader	Sigfox ID/PAC/AES key	Sigfox Verified AT command application
Uplynx SoC	✓	*	
Uplynx module BSM8001-0x	✓	✓	✓

**Table 6-1 Preloaded software in Uplynx products**

\*For SoC product, SoC can be shipped with ID/PAC/Key configuration files which can be flashed onto the SoC with users firmware. Details can refer to application note: Uplynx Products (Addendum – Project Development and Production Test)(AN-UPLYNX-002) and Uplynx Products (Addendum - Boot Procedure) (AN-UPLYNX-003)

## 7 System Top Register

### 7.1 Introduction

The system manager unit mainly controls system boot up, select pin function, pin configuration, software interrupt, additional SPI0 CS pins and the AGPIO configuration, which are described below. This unit also provides chip ID and device type as described below.

### 7.2 Multi-Function Pin

The Uplynx XS8001-T has 8 sets of analogue/digital multi-function pins and digital only multi-function pins. Each multi-function pin can be configured by the user. The definition is shown in the following table.

All the pins shared with EBI function will switch to EBI I/O. If EBI\_EN is disabled, the PINMUXx.GPIOx\_MUX select pin function of multi-function and peripherals.

The AGPIO functions as an analog and digital mux GPIO. It can be ACMP and SARADC source when the analog function is enabled. It also can be GPIO, EBI and GPIO reset. The function of each AGPIO is listed in the above table.

The analogue/digital function switches of the AGPIOs are defined in the AGPIO\_CTRL0 register.

If the user selects the GPIO0 function, then AGPIO\_CTRL0.AGPIO\_12\_AEN must be set to 0.

If AGPIO\_CTRL0.AGPIO\_12\_AEN is set to 1, the AGPIO1 function depends on AGPIO\_CTRL0.AGPIO1\_FUNC1 setting.

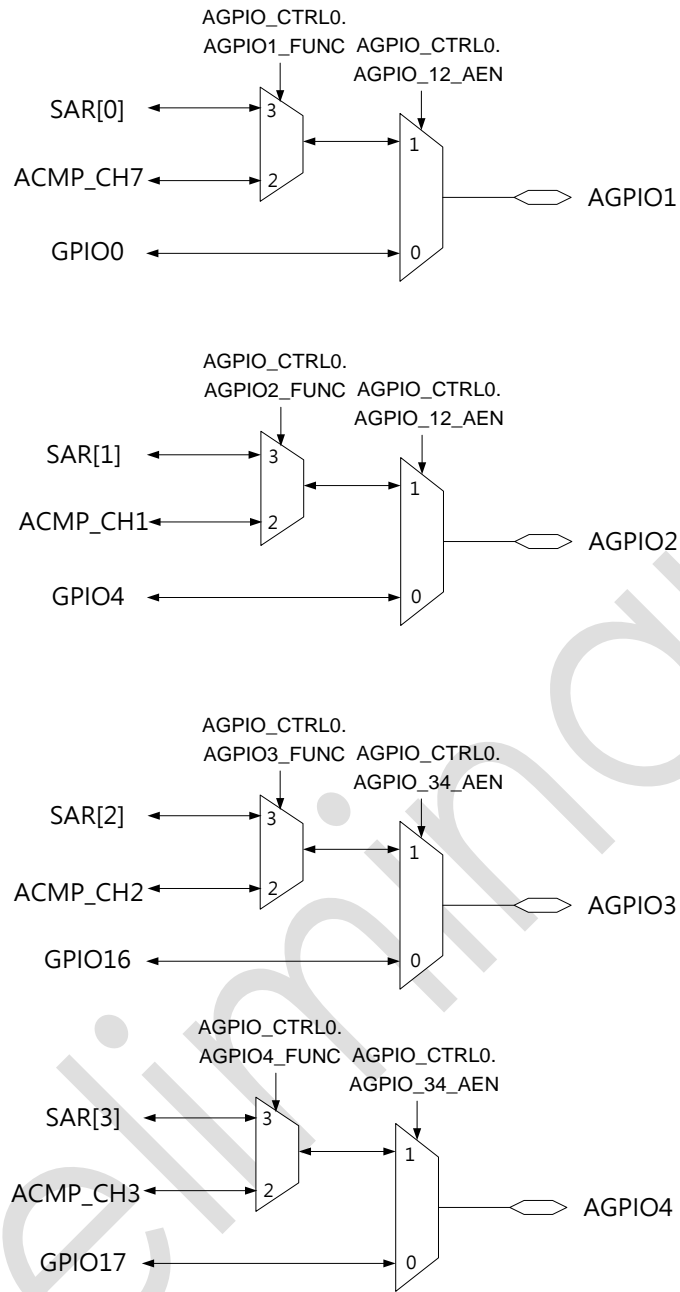


Figure 7-1 Block diagram of AGPIO {1-4}

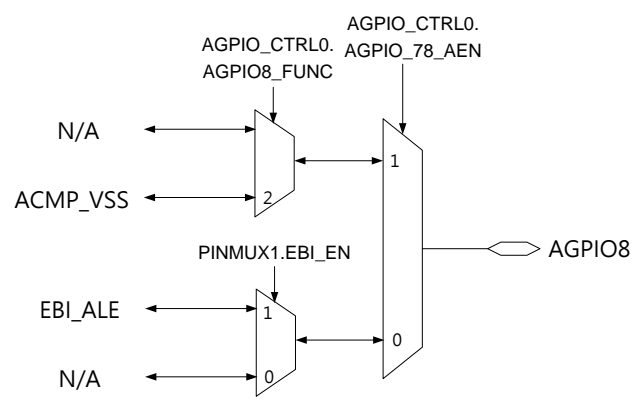
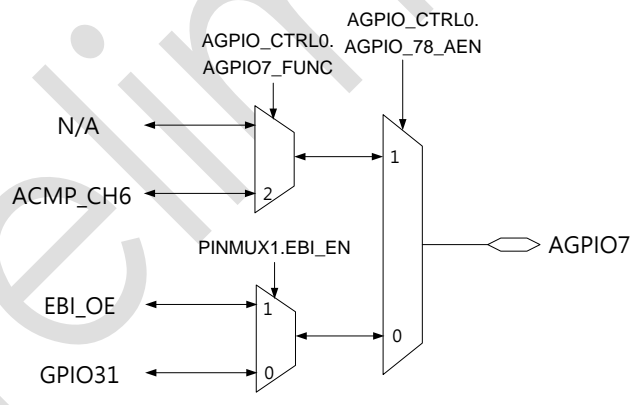
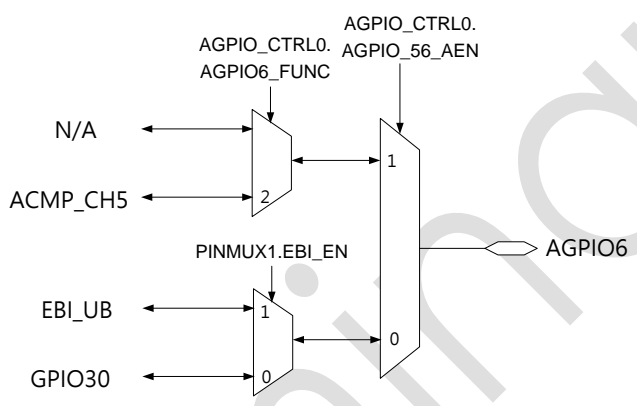
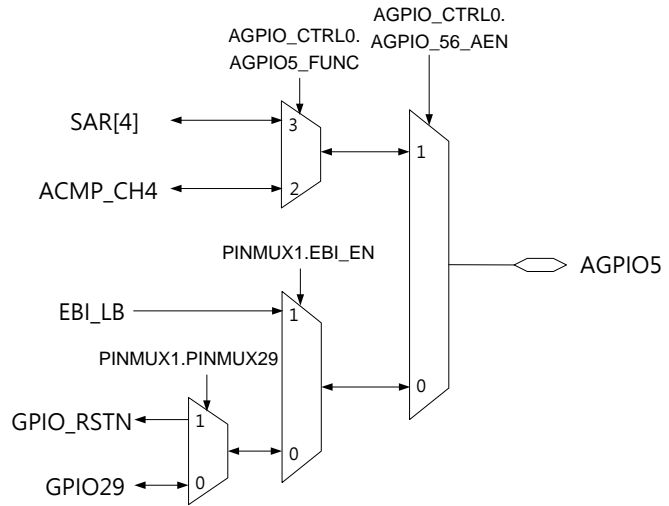


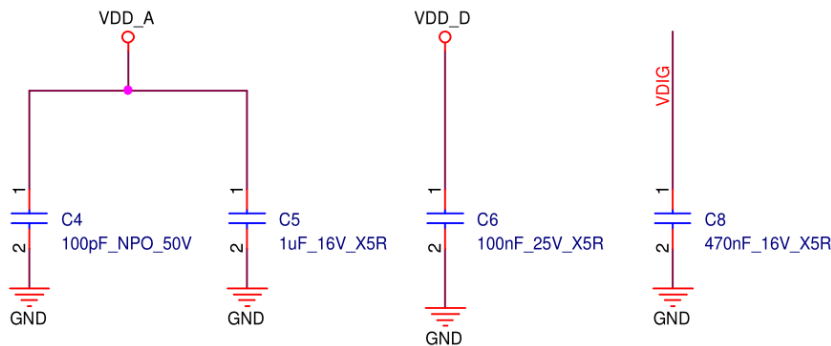
Figure 7-2 Block diagram of AGPIO {5-8}

## 8 Application Information

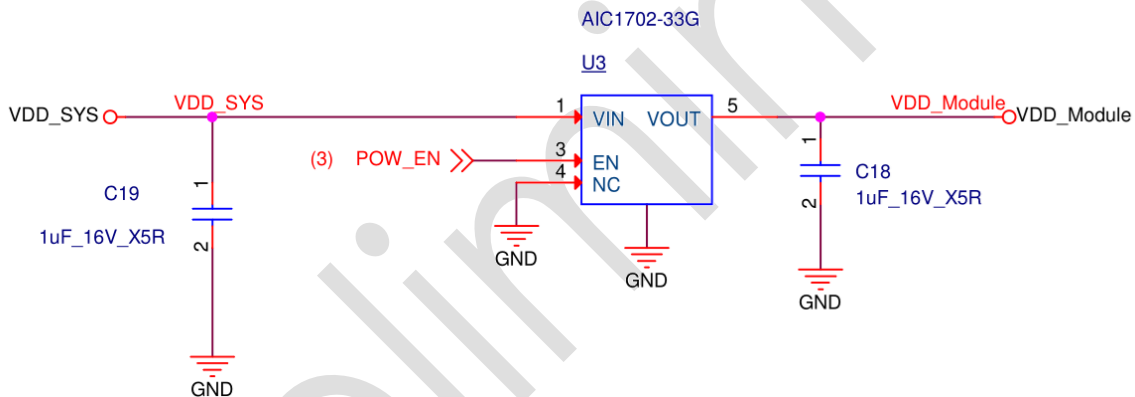
### 8.1 Sigfox RCZ1,2,3,4,5,6 Reference Circuit

#### 8.1.1 Uplynx XS8001-T Power Circuit

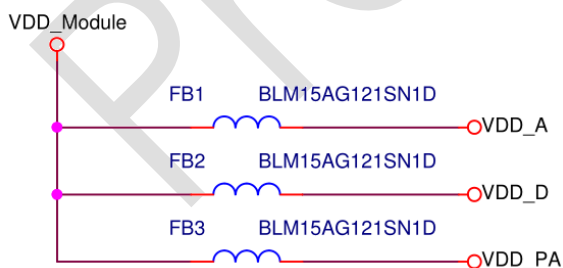
The Uplynx XS8001-T requires voltage to be supplied to pins 6, 46, 47 and 48. The decoupling circuit should be placed close to the SOC as suggested in the layout Gerber file.



**Figure 8-1 Power Decoupling Circuit**



**Figure 8-2 LDO Circuit**



**Figure 8-3 Beads between Power Domains**

Ferrite beads FB1, FB2 and FB3 are inserted to isolate the power domains VDD\_A, VDD\_D and VDD\_PA respectively from each other and to avoid unwanted noise coupling to the main power supply VDD\_module.

#### 8.1.2 Uplynx XS8001-T clock Circuit

The reference circuit consists of a 24MHz TCXO. A power gating PMOS (Q6) is used to gate off the current drawn when sleep mode is active. On powering on, TCXO\_PD is pulled low. The selection of C26 is to ensure proper operating point of XTAL\_OUT.

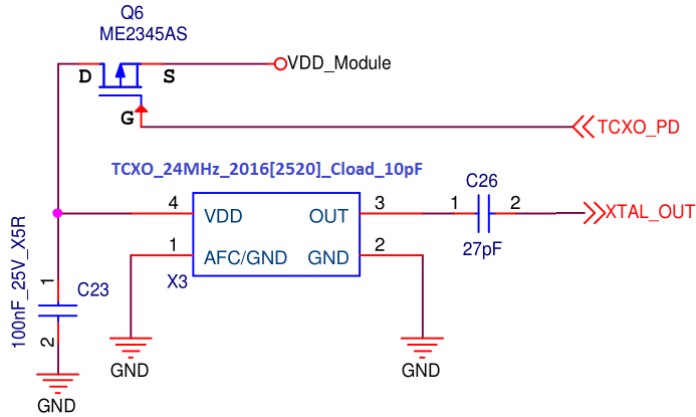


Figure 8-4 24MHz TCXO Circuit

8.1.3 Uplynx XS8001-T Control Circuit

The Uplynx XS8001-T is controlled by a dedicated power enabling pin POW\_EN. A high level state indicates power ON and low is OFF. When the module is ON, the Sigfox AT command interface is loaded automatically. UART\_TX and UART\_RX are the pins for the UART interface. AT command is configured for communication through this UART interface at 9600bps (no flow control, 8 data bit, 1 stop bit). The RESET is used to reset the SOC which is active low. A pull up resistor over a capacitor is included in the design as a means of resetting the SOC on startup.

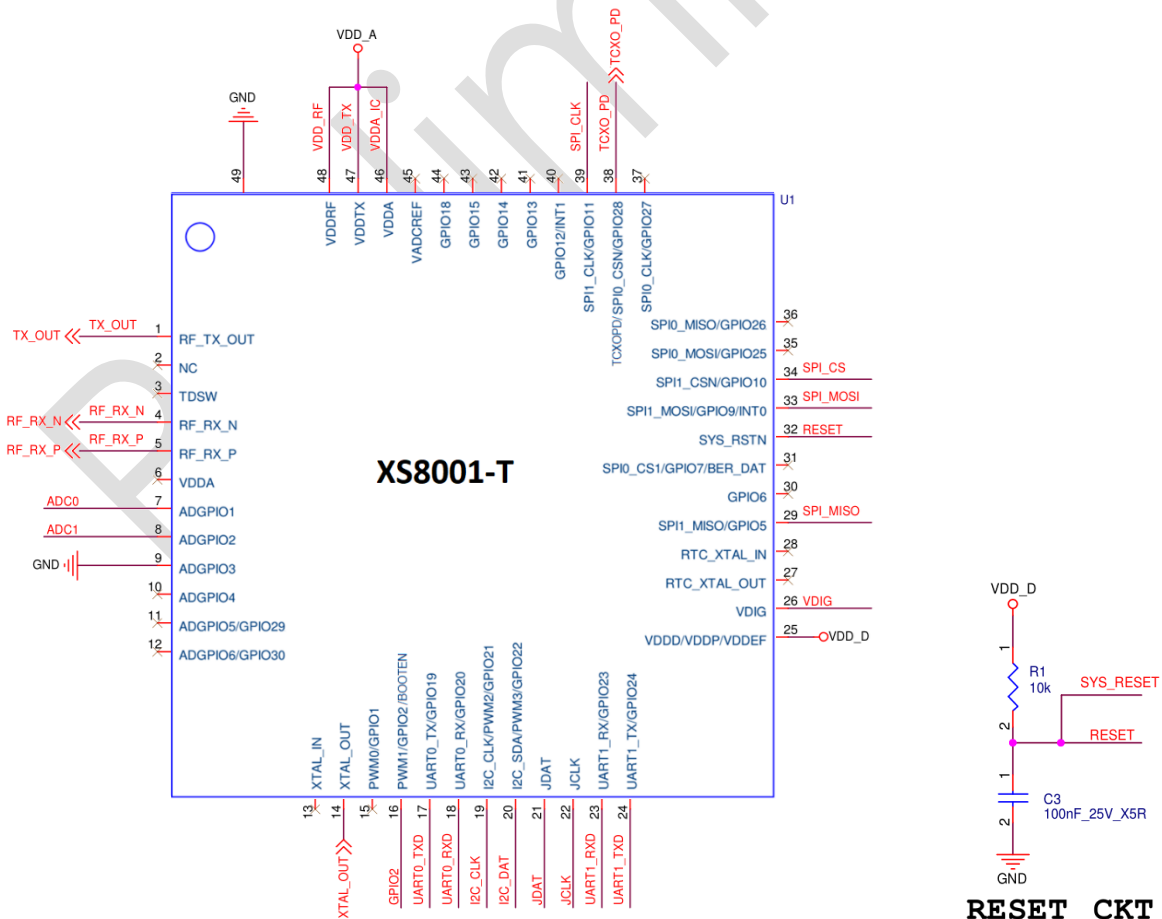


Figure 8-5 Control and Reset Circuit

8.1.4 Uplynx XS8001-T Radio Frequency Circuit

● RCZ1,2,3,4, 5 and 6 operation

The RF reference circuit consists of the matching and filter circuit for the power amplifier and low noise amplifier which covers the operating frequency of 868MHz, 902MHz to 920MHz which compliant with FCC (FCC-like), CE and ARIB T-108 regulatory requirements<sup>1</sup>.

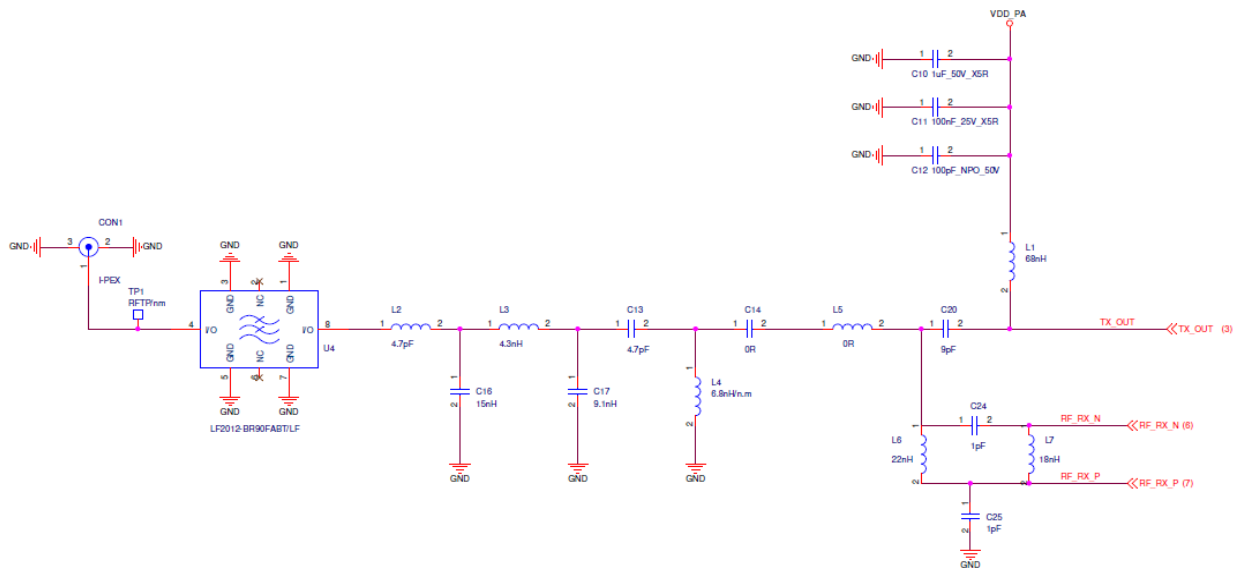


Figure 8-6 RCZ123456 Recommended Sigfox Ref. Design – RF Matching and Filtering Circuit

● RCZ3 , RCZ4 and RCZ5 operation

The RF reference circuit consists of the matching and filter circuit for the power amplifier and low noise amplifier. BSM8001-03 module is designed for the region with operating frequency of 902MHz to 920MHz which compliant with ARIB T-108 regulatory requirements<sup>2</sup>.

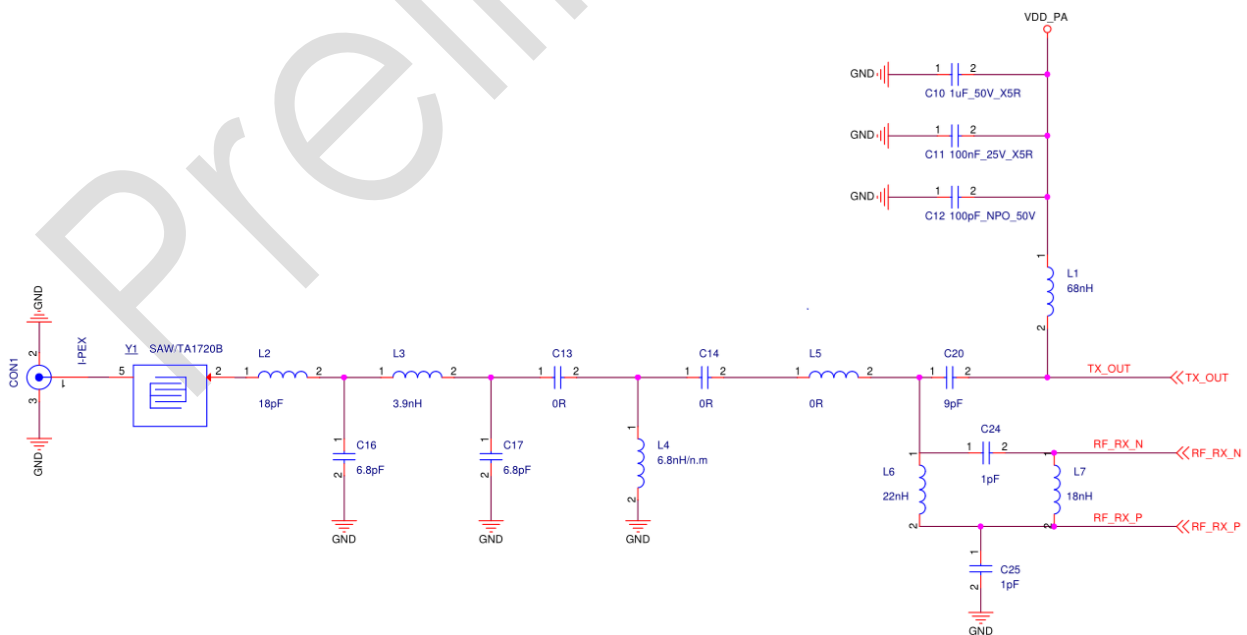


Figure 8-7 RCZ3 and RCZ5 Recommended Sigfox Ref. Design – RF Matching and Filtering Circuit

<sup>1</sup> Test reports can be made available upon request

<sup>2</sup> Test reports can be made available upon request

**9 Design-in options and Production flow**

To design with XS8001-T and XS8001-T for Sigfox product, there are three options

<i>Design-in Option</i>	<i>Application to Sigfox P1 certification program</i>	<i>ID/PAC/AES Key source</i>	<i>Preloaded Firmware</i>	<i>Suitable for</i>
<b>Chip on board</b> with application circuit <b>different</b> from Sigfox verified reference circuits	<b><u>New P1 application is needed</u></b>	Directly from <b>Sigfox</b> after P1 certification program	*Bootloader only	New product with special requirement on material, form factor
<b>Chip on board</b> with application circuit <b>identical</b> to that Sigfox verified reference circuits	<b><u>Not necessary</u></b> - ESMT Sigfox verified reference design is reused.	<b>ESMT</b> provides ID/PAC information and to be programmed during manufacturing process		Low cost system solution or solution targeted at minimal PCBA size
<b>Module on board</b>	<b><u>Not necessary</u></b> - ESMT Sigfox verified reference design is reused.	<b>Embedded</b> in the module	*Bootloader, ID/PAC and Sigfox verified AT command application firmware	All applications

\* Sigfox Verified AT command application firmware & firmware built based on ESMT SDK can be uploaded via Bootloader command

**9.1 Chip on Board manufacturing flow**

An application note “Uplynx Products (Addendum – Project Development and Production Test” described the procedure in details. Basically, the DUT needs to be tested for RF compliance, RF output power and the frequency offset and temperature sensor calibrated words are to be written into the flash area in the DUT at the end of the manufacturing test procedure. The complete production flow with XS8001-T and XS8001-T have been developed in LitePoint IQFlex and one may contact Sales and representatives of LitePoint.

**9.2 Module on Board**

Every module is tested thoroughly before shipment, simple RF packet power and frequency offset test would be enough to ensure proper operation.

**10 Order Information.**

Product Name	Order Part Number	Description
XS8001-T Sigfox System on Chip support for RCZ123456	XS8001-T	High performance Wireless MCU with Sigfox uplink with Sigfox RC123456

Preliminary