Uplynx XS8001-T-NG48NRY SOC Datasheet

ESDS-UPLYNX-007 Version 1.3

ESMT Inc.

Important Notice

Trademarks

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Revision Control

Ver.	Date	Description of Change	Approved
1.0	23/8/2018	Document First version	Charles Lee
1.1	1/10/2018	Production and Packaging Information	Charles Lee
1.2	1/11/2018	IC marking change	Charles Lee
1.3	1/17/2018	Part number amendment	Charles Lee

Table of Contents

List of Figures

List of Tables

1 *Product Overview*

The Uplynx XS8001-T-NG48NRY is one of ESMTs family of wireless SOCs designed for ultra-low-power wireless IoT applications.

The Uplynx XS8001-T-NG48NRY monolithically integrates the Sigfox protocol stack with best-in-class sub-GHz RF performance.

The Uplynx XS8001-T-NG48NRY 's built-in 10-bit ADC, analogue comparators and GPIOs are available for access via an AT command set over UART interface.

The Uplynx XS8001-T-NG48NRY is the most cost effective, smallest, and easy-to-design SOC solution for IoT applications where wireless data uplink is enabled via the Sigfox network.

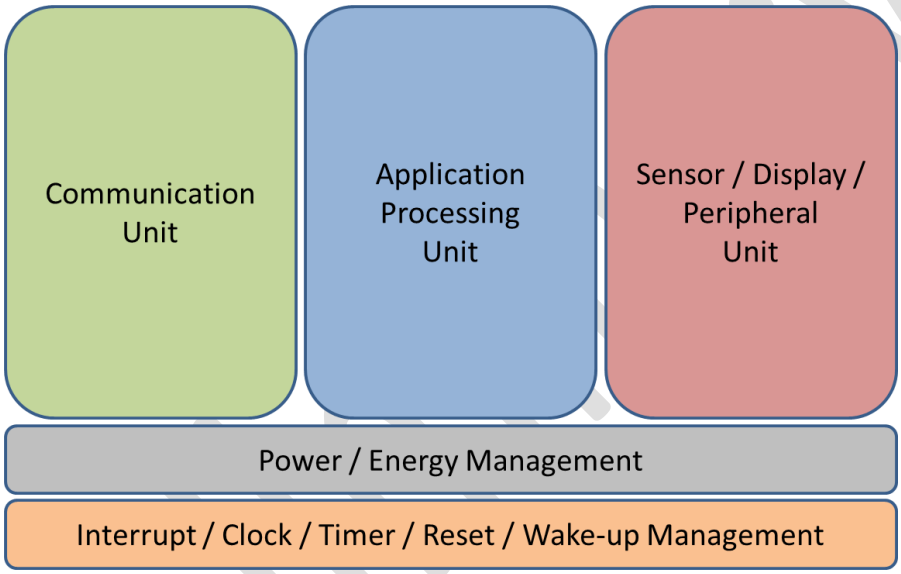


Figure 1-1 Functional Blocks

2 *Product Features*

2.1 *Communication Unit*

- 868 (863~870) MHz, 870-875.6MHz, 915 (902-928) MHz ISM band support
- State-of-the-art integrated RF front-end with high-performance synthesizer and integrated power amplifier
- Programmable PA output power up to 22dBm
- Sigfox™ uplink compliant RF signaling via tight Power Amplifier profiling and phase shaping
- Sigfox Verified™ reference circuit for RCZ1,2,3,4 (5,6) AT command set
- Build in channel power detector for LBT implementation

2.2 *Application Processing Unit*

- ANDES 32-bit AndesCore N801-S processor
- Energy-Efficient
- Programmable up to 60MHz
- Up to 128kB embedded FLASH
- 8kB Instruction RAM for time-critical tasks or data memory extension
- Up to 24kB Data RAM with retention
- Supports 10-channel Direct Memory Access (DMA)
- AES-128 ciphering and deciphering hardware engine with CCM support
- Arithmetic coding engine for data compression/decompression

2.3 *Sensor / Display / Peripheral Unit*

- GPIOs for general peripheral support
- SPI, I2C, UART,
- 2x 32-bits PWM Engines with two channels each
- 4-channel 10-bit on-chip ADC for external analog sources
- Embedded on-chip monolithic temperature sensor
- Low-power analog comparator with wake-up support
- Programmable supply detect alarm (AVDD) for battery monitoring

2.4 *Interrupt / Clock / Timer / Reset / Wake-up Management*

- Built-in power-on-reset (POR)
- On-chip low-power 32kHz oscillator
- Integrated 12MHz crystal oscillator driver, support external 24MHz TCXO
- Fine-grain dynamic PLL frequency setting for optimal power / performance
- Real-Time-Clock (RTC)
- Watch-Dog Timer (WDT)
- 3x 32-bit general-purpose fast timer
- 3x 32-bit ultra-low-power timers with wake-up support

2.5 *Power / Energy Management*

- VDD = 2.5V – 3.5V (Sigfox verified reference design at 2.5V and 3.3V for RCZ1 and RCZ2/4 respectively)
- Operating temperature -40°C to 85°C
- Multiple internal LDOs for supply noise immunity and optimized performance
- Sigfox Tx mode: Typically 58mA at 14dBm output (Tx + Sigfox AT uplink modem)
- Integrated power management engine to optimize energy consumption
    - *Normal* mode: full features with clock speed up to 60MHz
    - *Idle* mode: Normal mode with CPU clock-gated for power-saving
    - *Sleep* mode: System in hibernate except SRAM and partial digital register bank in retention for fast wake-up

2.6 *Small Form-Factor*

- Available in 7mm x 7mm 48-pin QFN package
- Compact board design with very low external component count

2.7 *Easy-to-Design*

- The Uplynx XS8001-T-NG48NRY comes with a complete set of technical documents. They include basic product briefs, datasheets, technical reference manuals as well as many application notes.
- The Uplynx XS8001-T-NG48NRY comes with a baseboard for development and/or evaluation.

3 *Functional Block*

Shown below is the functional block diagram for the 48-pin version of the Uplynx XS8001-T-NG48NRY , which includes an EBI (external bus interface), used to implement additional memory on board, e.g. pseudo SRAM.

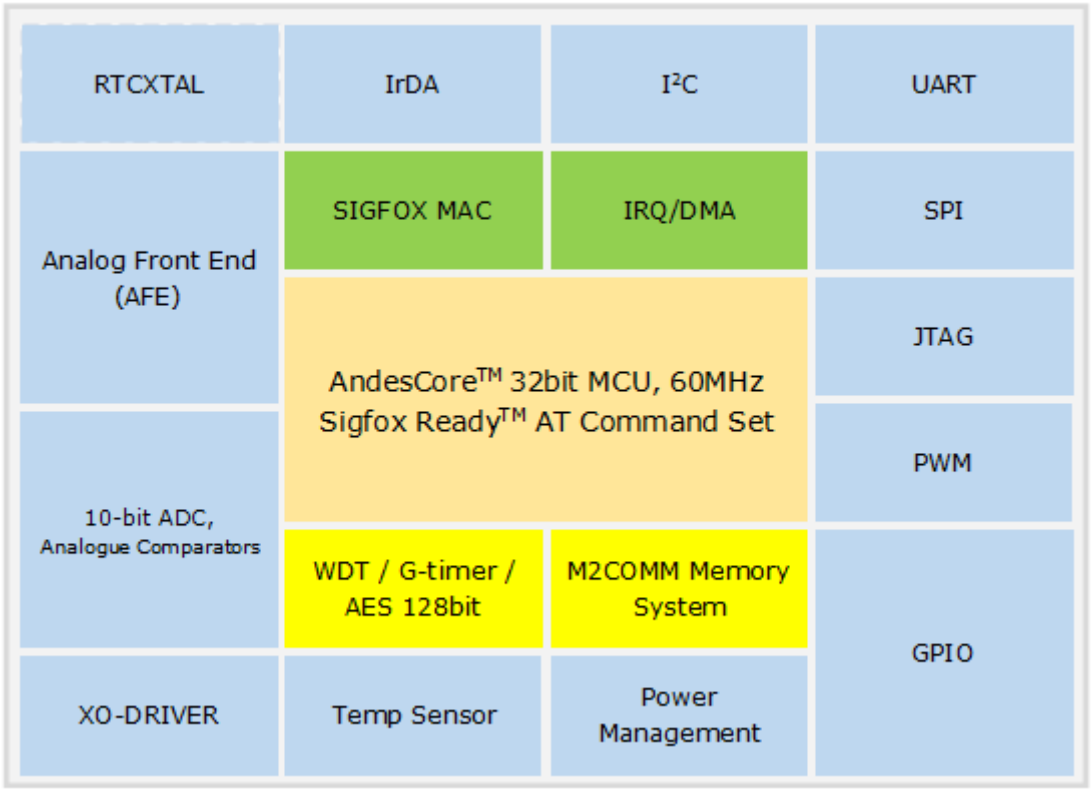


Figure 3-1 Functional Block Diagram

4 *Pin-out and package mechanicals*

4.1 *QFN48 Pinout*

Pin Number	Pin Name	Pin Type	Description
1	RF_TX_OUT	A	RF Power Amplifier Output
2	NC		Not used
3	TDSW		Not used.
4	RF_RX_N	A	LNA N- input
5	RF_RX_P	A	LNA P- input
6	VDDA	P	Analog 3.3V decoupling pin (Direct connection to main power is NOT a must)
7	ADGPIO1	A	Analog input to analog comparator channel 7 [ACMP_CH7]
		A	Analog input to MADC channel 1 [SAR_CH1] (0~2.5V)
	GPIO0	I/O	General purpose digital I/O pin [GPIO0]. See GPIO section for a complete description.
8	ADGPIO2	A	Analog input to analog comparator channel 1 [ACMP_CH1]
		A	Analog input to MADC channel 2 [SAR_CH2] (0~2.5V)
	GPIO4	I/O	General purpose digital I/O pin [GPIO4]. See GPIO section for a complete description.
9	ADGPIO3	I	Calibration use , this pin must be connected to system ground
10	ADGPIO4	A	Analog input to analog comparator channel 3 [ACMP_CH3]
		A	Analog input to MADC channel 5 [SAR_CH5] (0~1.2V)
	GPIO17	I/O	General purpose digital I/O pin [GPIO17]. See GPIO section for a complete description.
11	ADGPIO5	A	Analog input to analog comparator channel 4 [ACMP_CH4]
		A	Analog input to MADC channel 6 [SAR_CH6] (0~1.2V)
	GPIO29	I/O	General purpose digital I/O pin [GPIO29]. See GPIO section for a complete description.
12	ADGPIO6	A	Analog input to analog comparator channel 5 [ACMP_CH5]
	GPIO30	I/O	General purpose digital I/O pin [GPIO30]. See GPIO section for a complete description.
13	XTAL_IN	A	Crystal oscillator input
14	XTAL_OUT	A	Crystal oscillator output
15	GPIO1	I/O	General purpose digital I/O pin [GPIO1]. See GPIO section for a complete description.
	PWM0	O	PWM0 channel 0 output
16	GPIO2	I/O	General purpose digital I/O pin [GPIO2]. See GPIO section for a complete description.
	BOOTEN	I	When it is pulled low at power up, the bootloader is initiated. Refer to Uplynx Products (Addendum - Boot Procedure) (AN-UPLYNX-003).pdf for details
	PWM1	O	PWM0 channel 1 output
17	UART0_TX	O	UART0 data transmitter output pin
	GPIO19	I/O	General purpose digital I/O pin [GPIO19]. See GPIO section for a complete description.
18	UART0_RX	I	UART0 data receiver input pin
	GPIO20	I/O	General purpose digital I/O pin [GPIO20]. See GPIO section for a complete description.

Pin Number	Pin Name	Pin Type	Description
19	I2C_CLK	O	I2C clock pin
	GPIO21	I/O	General purpose digital I/O pin [GPIO21]. See GPIO section for a complete description.
	PWM2	O	PWM1 channel 0 output
20	I2C_SDA	I/O	I2C data I/O pin
	GPIO22	I/O	General purpose digital I/O pin [GPIO22]. See GPIO section for a complete description.
	PWM3	O	PWM1 channel 1 output
21	JDAT	I/O	JTAG data I/O pin
22	JCLK	I	JTAG clock pin
23	UART1_RX	I	UART1 data receiver input pin
	GPIO23	I/O	General purpose digital I/O pin [GPIO23]. See GPIO section for a complete description.
24	UART1_TX	O	UART1 data transmitter output pin
	GPIO24	I/O	General purpose digital I/O pin [GPIO24]. See GPIO section for a complete description.
25	VDDD	P	Digital power
26	VDIG	A	Core voltage
27	RTC_XTAL_OUT	A	32KHz crystal oscillator output
28	RTC_XTAL_IN	A	32KHz crystal oscillator input
29	GPIO5	I/O	General purpose digital I/O pin [GPIO5]. See GPIO section for a complete description.
	SPI1_MISO	I/O	SPI1 master in / slave out pin.
30	GPIO6	I/O	General purpose digital I/O pin [GPIO6]. See GPIO section for a complete description.
31	GPIO7	I/O	General purpose digital I/O pin [GPIO7]. See GPIO section for a complete description.
	SPI0_CS1	O	SPI0 second chip select pin
32	SYS_RSTN	I	System reset pin – Active Low
33	GPIO9	I/O	General purpose digital I/O pin [GPIO9]. See GPIO section for a complete description. Not recommended as interrupt source
	SPI1_MOSI	I/O	SPI1 master out / slave in pin
	-	I	-
34	SPI1_CSN	O	SPI1 chip select pin
	GPIO10	I/O	General purpose digital I/O pin [GPIO10]. See GPIO section for a complete description.
35	SPI0_MOSI	I/O	SPI0 master out / slave in pin
	GPIO25	I/O	General purpose digital I/O pin [GPIO25]. See GPIO section for a complete description.
36	SPI0_MISO	I/O	SPI0 master in / slave out pin
	GPIO26	I/O	General purpose digital I/O pin [GPIO26]. See GPIO section for a complete description.
37	SPI0_CLK	O	SPI0 clock pin
	GPIO27	I/O	General purpose digital I/O pin [GPIO27]. See GPIO section for a complete description.

Pin Number	Pin Name	Pin Type	Description
38	SPI0_CSN0	O	SPI0 first chip select pin
	GPIO28	I/O	General purpose digital I/O pin [GPIO28]. See GPIO section for a complete description.
	TCXO_PD	O	Power down signal for TCXO
39	SPI1_CLK	O	SPI1 clock pin
	GPIO11	I/O	General purpose digital I/O pin [GPIO11]. See GPIO section for a complete description.
40	GPIO12	I/O	General purpose digital I/O pin [GPIO12]. See GPIO section for a complete description. Not recommended as interrupt source
	-	I	-
41	GPIO13	I/O	General purpose digital I/O pin [GPIO13]. See GPIO section for a complete description.
42	GPIO14	I/O	General purpose digital I/O pin [GPIO14]. See GPIO section for a complete description.
43	GPIO15	I/O	General purpose digital I/O pin [GPIO15]. See GPIO section for a complete description.
44	CAPCHGE	O	LDO pre-charge/pre-discharge
45	VADCREF		Not used
46	VDDA	P	Analog power
47	VDDTX	P	Analog power
48	VDDRF	P	Analog power

Table 4-1 XS8001-NG48NRY /XS8001-T-NG48NRY QFN48 Pin Designations

Pin Type	Description
O	Digital Output Pin
I	Digital Input Pin
A	Analog Pin
G	Ground Pin
P	Power Pin

Table 4-2 Pin Type Description

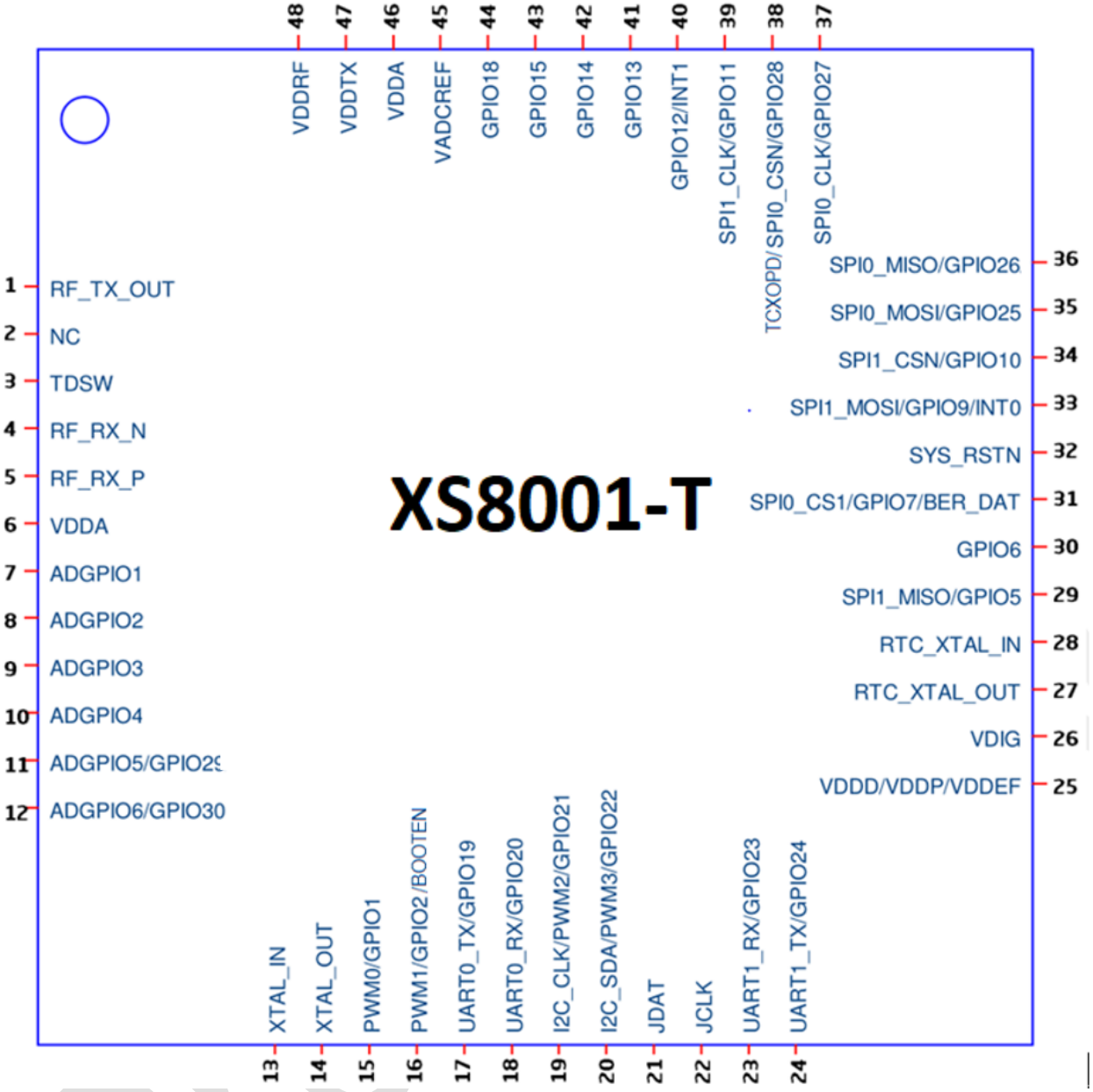
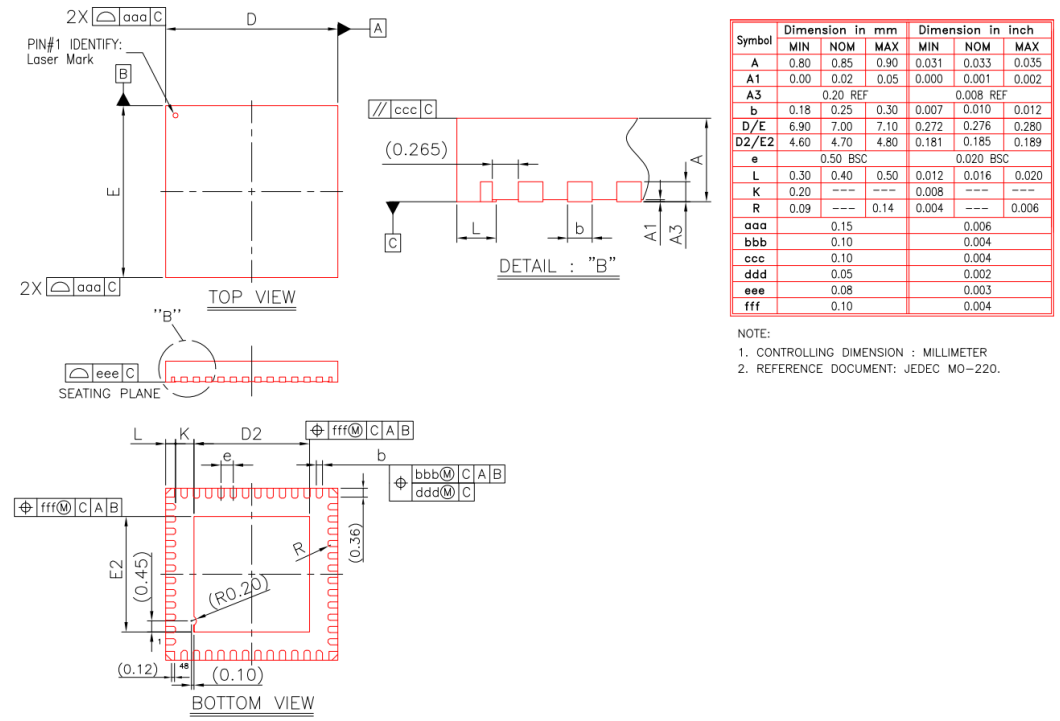


Figure 4-1 Uplynx XS8001-NG48NRY and XS8001-T-NG48NRY symbol(QFN48)

4.2 48-pin QFN Package Outline



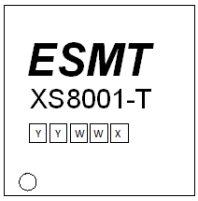
Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3		0.20 REF			0.008 REF	
b	0.18	0.25	0.30	0.007	0.010	0.012
D/E	6.90	7.00	7.10	0.272	0.276	0.280
D2/E2	4.60	4.70	4.80	0.181	0.185	0.189
e		0.50 BSC			0.020 BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020
K	0.20	---	---	0.008	---	---
R	0.09	---	0.14	0.004	---	0.006
aaa		0.15			0.006	
bbb		0.10			0.004	
ccc		0.10			0.004	
ddd		0.05			0.002	
eee		0.08			0.003	
fff		0.10			0.004	

NOTE:
1. CONTROLLING DIMENSION : MILLIMETER
2. REFERENCE DOCUMENT: JEDEC MO-220.

Figure 4-2 XS8001-NG48NRY /XS8001-T-NG48NRY QFN-48 Package Outline

4.3 *XS8001-T-NG48NRY Marking*

Part Number: XS8001-T-NG48NRY



Item	Value
Marking Type	Laser
Line 1	Logo
Line 2	Product reference: XS8001-T
Line 3 [YY WW X]	Date Code : YY- Year, WW – Week, X - reserved

5 *Electrical Specifications*

Parameter	Note	Min	Max	Unit
RF/Analogue Domain Power (VDDA, VDDRF, VDDD)		-0.3	3.5	V
Voltage on PA_OUT	DC		3.5	V
Voltage on GPIO/ADGPIO		-0.3	3.5	V
Voltage on XO12M, XI12M, XO32k and XI32k		-0.3	1.5	V
Voltage on GPIO as input		-0.3	3.5	V
Storage Temperature		-40	140	°C

Table 5-1 Absolute Maximum Ratings

Parameter	Min	Typ.	Max	Unit
RF/Analogue Domain Power (VDDA, VDDRF, VDDD)	2.5		3.5	V
Operating Temperature	-40		85	°C

Table 5-2 Recommended Operating Conditions

Parameter	Note	Min	Typ.	Max	Unit
ESD (human body model)	All pin			±2000	V
ESD (charged device model)	All pin			±500	V
ESD (machine model)	Non-RF Pin			±200	V
ESD (machine model)	RF Pin (1)			+150	V

(1) TX, X0_IN, X0_OUT

Table 5-3 Environmental Characteristics

Parameter	Note	Min	Typ.	Max	Unit
Sleep mode RC oscillator enabled			7		µA
Sigfox RCZ1 Tx mode 868MHz 14dBm @ 3.3V*			65		mA
Sigfox RCZ2 Tx mode 902MHz 22dBm @ 3.3V*			130		mA
Sigfox RCZ3 Tx mode 923MHz 12dBm @ 3.3V*			65		mA
Sigfox RCZ4 Tx mode 923MHz 14dBm @ 3.3V*			140		mA
Sigfox RCZ5 Tx mode 923MHz 13dBm @ 3.3V*			tbd		
*Average Current measured during Sigfox packet transmission.					

Table 5-4 DC Current Characteristics

Parameter	Condition/Note	Min	Typ.	Max	Unit
Output power (VDD=3.3V)	1dBm step between 7~22dBm	7		23	dBm
Power step size	from 7dBm to 22dBm	0.5	1		dB

Table 5-5 Transmitter RF Performance

Parameter	Min	Typ.	Max	Unit
Reference Frequency		12/24		MHz
Frequency Range	778		960	MHz

Table 5-6 Synthesizer Specification

Parameter	Note	Min	Typ.	Max	Unit
Calibrated frequency	±5% course calibration		32.768		kHz
Frequency accuracy after calibration	With software offset adjustment routine			±1	%
Supply voltage coefficient	Frequency drift when supply voltage changes after calibration		+10		%/V
Initial calibration time			2.5		ms

Table 5-7 32kHz RC Oscillator Specification

Parameter	Condition/Note	Min	Typ.	Max	Unit
Crystal frequency			32.768		kHz
Load capacitance			14		pF
Tolerance			±20		ppm
Start-up time			400		ms

Table 5-8 32kHz Crystal Oscillator Specification

Parameter	Condition/Note	Min	Typ.	Max	Unit
Operating voltage		0		VDD	
THD (Total Harmonic Distortion)	DC at VDDA/2 , signal amplitude = 500mV		70		dB
Signal Frequency		0		500	kHz

Table 5-9 Analogue Multiplexer Specification (MADC/ACMP channel)

Parameter	Condition/Note	Min	Typ.	Max	Unit
Input Voltage		0.1		VDD-0.1	V
Hysteresis	mode 1		±5		mV
	mode 2		±20		mV
	mode 3		±35		mV
	mode 4		±45		mV
Settling Time			135		us
Internal Reference (VDDA scalar)		2/33		30/33	VDD
Internal Reference (potential difference across an internal resistor with a fix current)		190		960	mV

Table 5-10 Analogue Comparator ACMP0 / ACMP1 Specification

Parameter	Condition/Note	Min	Typ.	Max	Unit
Battery Voltage tipping point	Configurable [1.6V, 1.8V, 2V and 2.5V]	1.6	1.8	2.5	V

Table 5-11 Battery Monitor Specification

Parameter	Condition/Note	Min	Typ.	Max	Unit
Temperature range		-20	25	80	°C
Un-calibrated Temperature Error			±20		°C
Calibrated Temperature Error			±5		°C

Table 5-12 Temperature Sensor Specification

Parameter	Condition/Note	Min	Typ.	Max	Unit
Resolution			10		Bit
AVDD Range			1.8 - 3.5		V
Full Scale	AVDD >3.0		2.5		V
Full Scale	AVDD <3.0		1.2		V
Clock Rate				3	MHz
Conversion Rate				250	kHz
Input Impedance	1MHz		9		MΩ
Input Impedance	100kHz		1		MΩ
Input Impedance	10kHz		0.1		MΩ

Table 5-13 Monitoring ADC Specification

6 *Preloaded Software*

The Uplynx products are loaded with the following software prior shipping:

Product	Bootloader	Sigfox ID/PAC/AES key	Sigfox Verified AT command application
Uplynx SoC	✓	*	
Uplynx module BSM8001-0x	✓	✓	✓

Table 6-1 Preloaded software in Uplynx products

*For SoC product, SoC can be shipped with ID/PAC/Key configuration files which can be flashed onto the SoC with users firmware. Details can refer to application note: Uplynx Products (Addendum – Project Development and Production Test)(AN-UPLYNX-002) and Uplynx Products (Addendum - Boot Procedure) (AN-UPLYNX-003)

7 *System Top Register*

7.1 *Introduction*

The system manager unit mainly controls system boot up, select pin function, pin configuration, software interrupt, additional SPI0 CS pins and the AGPIO configuration, which are described below. This unit also provides chip ID and device type as described below.

7.2 *Multi-Function Pin*

The Uplynx XS8001-T-NG48NRY has 8 sets of analogue/digital multi-function pins and digital only multi-function pins. Each multi-function pin can be configured by the user. The definition is shown in the following table.
All the pins shared with EBI function will switch to EBI I/O. If EBI_EN is disabled, the PINMUXx.GPIOx_MUX select pin function of multi-function and peripherals.

N2 (QFN48) PIN Number	EBI_EN=0 & GPIOx_MUX=0	EBI_EN=0 & GPIOx_MUX=1	EBI_EN=0 & GPIOx_MUX=2
7	GPIO0		
8	GPIO4		
9	GPIO16		
10	GPIO17		
11	GPIO29	GPIO_RSTN	
12	GPIO30		
15	GPIO1	PWM0.0	
16	GPIO2	PWM0.1	
17	UART0_TX	GPIO19	
18	UART0_RX	GPIO20	
19	I2C_CLK	GPIO21	PWM1.0
20	I2C_SDA	GPIO22	PWM1.1
21	JDAT		
22	JCLK		
23	UART1_RX	GPIO23	
24	UART1_TX	GPIO24	
29	GPIO5	SPI1_MISO	
30	GPIO6		
31	GPIO7	SPI0_CSN1	
32	GPIO8		
33	GPIO9	SPI1_MOSI	EXT_INT0
34	GPIO10	SPI1_CSN	CLK0_O
35	SPI0_MOSI	GPIO25	
36	SPI0_MISO	GPIO26	
37	SPI0_CLK	GPIO27	
38	SPI0_CSN0	GPIO28	

N2 (QFN48) PIN Number	EBI_EN=0 & GPIOx_MUX=0	EBI_EN=0 & GPIOx_MUX=1	EBI_EN=0 & GPIOx_MUX=2
39	GPIO11	SPI1_CLK	
40	GPIO12	EXT_INT1	CLK1_O
41	GPIO13		
42	GPIO14		
43	GPIO15		

Table 7-1 Configuration of Digital Multi-function Pins

N2 (QFN48) PIN number	AGPIOx_AEN = 1 & AGPIOx.FUNC=2'b10	AGPIOx_AEN = 1 & AGPIOx.FUNC=2'b11	AGPIOx_AEN = 0
7	ACMP_CH[7]	SAR_CH[1]	GPIO0
8	ACMP_CH[1]	SAR_CH[2]	GPIO4
10	ACMP_CH[3]	SAR_CH[5]	GPIO17
11	ACMP_CH[4]	SAR_CH[6]	GPIO29/GPIO_RSTN/ EBI_LB
12	ACMP_CH[5]		GPIO30/EBI_UB

Table 7-2 Configuration of Mixed-mode Multi-function Pins via AGPIO

The AGPIO functions as an analog and digital mux GPIO. It can be ACMP and SARADC source when the analog function is enabled. It also can be GPIO, EBI and GPIO reset. The function of each AGPIO is listed in the above table.

The analogue/digital function switches of the AGPIOs are defined in the AGPIO_CTRL0 register.

If the user selects the GPIO0 function, then AGPIO_CTRL0.AGPIO_12_AEN must be set to 0.

If AGPIO_CTRL0.AGPIO_12_AEN is set to 1, the AGPIO1 function depends on AGPIO_CTRL0.AGPIO1_FUNC1 setting.

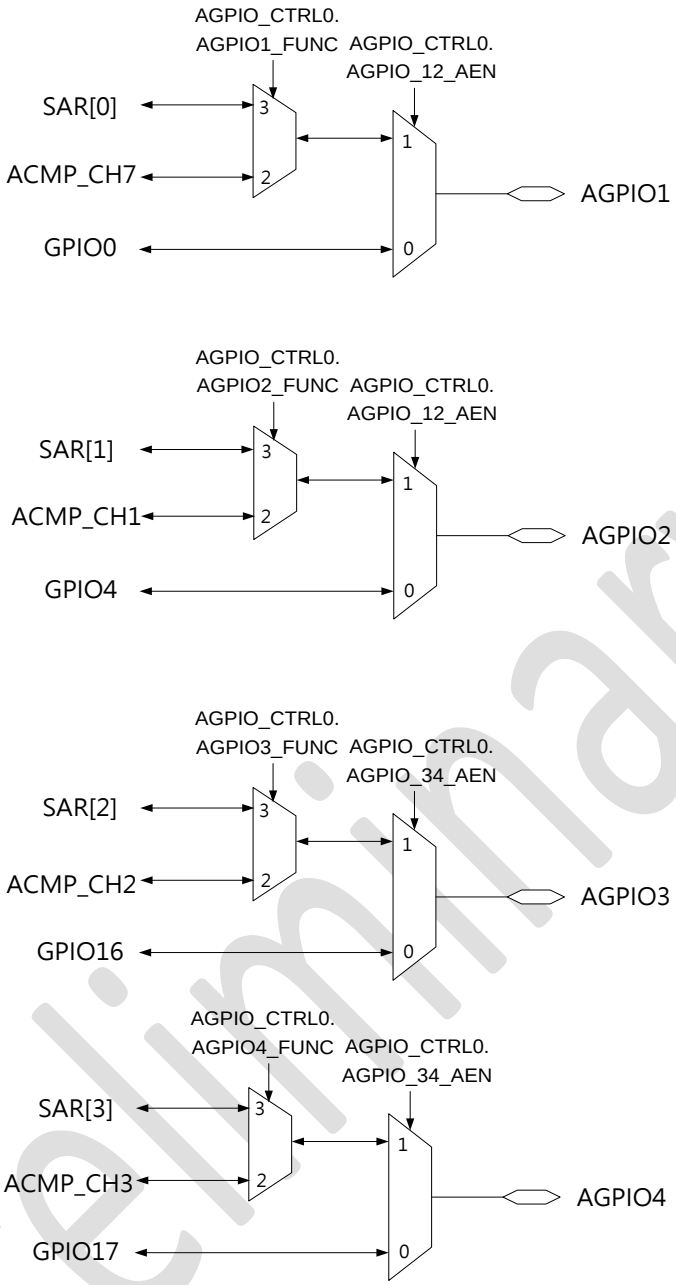


Figure 7-1 Block diagram of AGPIO {1-4}

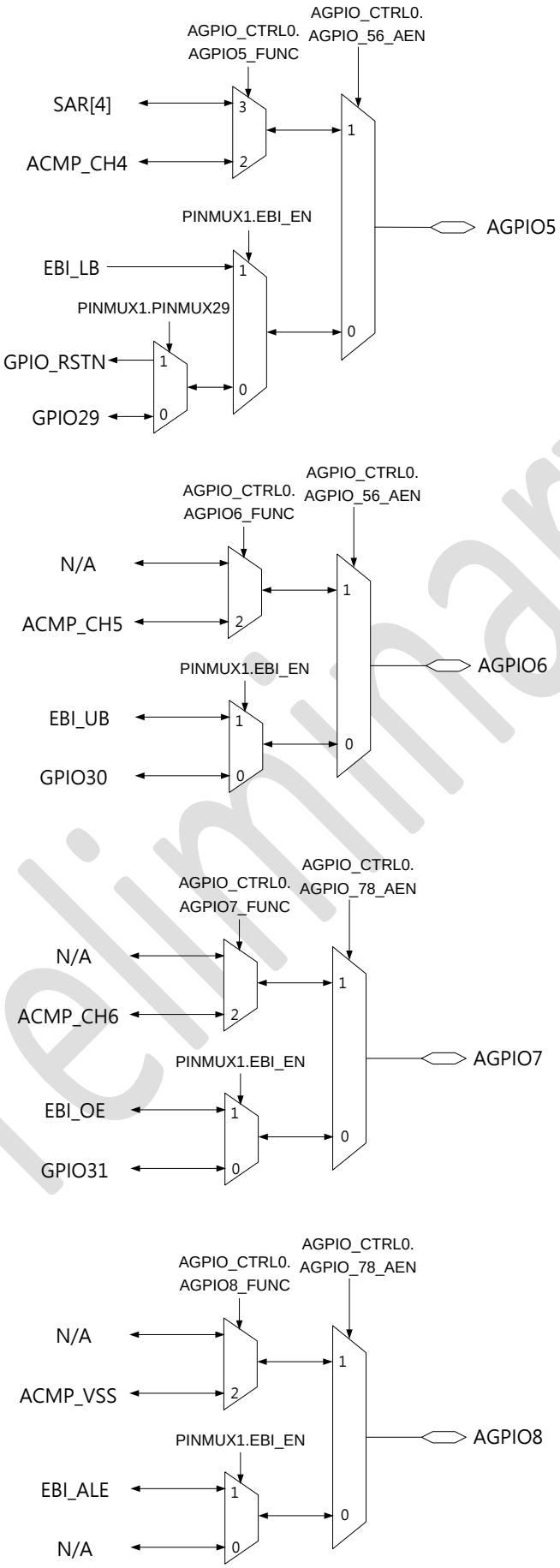


Figure 7-2 Block diagram of AGPIO {5-8}

7.3 Programming Model

7.3.1 Control Register Specification

Address	Type	Description	Reset value
+0x0C	R	ASIC version register	0x1408_1904
+0x14	R/W	Miscellaneous register	0x0000_0000
+0x20	R/W	PINMUX0 register	0x0000_0000
+0x24	R/W	PINMUX1 register	0x4000_0000
+0x54	R/W	GPIO_PE register	0x0000_0000
+0x60	R/W	AGPIO_CTRL0 register	0x0000_0000

Table 7-3 System Control Register Specification

7.3.2 ASIC version register

Bit	Name	Type	Description
31-24	YEAR	R	Year of ASIC version
23-16	MONTH	R	Month of ASIC version
15-8	DATE	R	Data of ASIC version
7-0	NUM	R	Number of ASIC version

Table 7-4 ASIC Version Register

7.3.3 Miscellaneous Register

Bit	Name	Type	Description
31-8		R/W	Reserved
7	SW_IRQ1	R/W	The bit indicates software IRQ1. 0x0: LOW, 0x1: HIGH
6	SW_IRQ0	R/W	The bit indicates software IRQ0. 0x0: LOW, 0x1: HIGH
5	SW_FIQ1	R/W	The bit indicates software FIQ1. 0x0: LOW, 0x1: HIGH
4	SW_FIQ0	R/W	The bit indicates software FIQ0. 0x0: LOW, 0x1: HIGH
3-1		R/W	Reserved
0	SPI0_CSN1	R/W	The bit used to be another CS signal of SPI0. It shows in GPIO7 pin. 0x0:LOW, 0x1:HIGH

Table 7-5 Miscellaneous Register

7.3.4 PINMUX0 Register

Bit	Name	Type	Description
31-30	GPIO15_MUX	R/W	0x0:GPIO15
29-28	GPIO14_MUX	R/W	0x0:GPIO14
27-26	GPIO13_MUX	R/W	0x0:GPIO13
25-24	GPIO12_MUX	R/W	0x0:GPIO12, 0x1:EXT_INT1, 0x2: CLK1_O
23-22	GPIO11_MUX	R/W	0x0: GPIO11, 0x1:SPI1_CLK,
21-20	GPIO10_MUX	R/W	0x0:GPIO10, 0x1:SPI1_CSN, 0x2: CLK0_O
19-18	GPIO9_MUX	R/W	0x0:GPIO9, 0x1:SPI1_MOSI, 0x2:EXT_INT0
17-16		R	Reserved
15-14	GPIO7_MUX	R/W	0x0:GPIO7, 0x1:SPI0_CSN1
13-12	GPIO6_MUX	R/W	0x0:GPIO6
11-10	GPIO5_MUX	R/W	0x0:GPIO5, 0x1:SPI1_MISO
9-8		R	Reserved
7-6	GPIO3_MUX	R/W	0x0:GPIO3
5-4	GPIO2_MUX	R/W	0x0:GPIO2, 0x1:PWM0.1
3-2	GPIO1_MUX	R/W	0x:GPIO1, 0x1:PWM0.0
1-0		R	Reserved

Table 7-6 PINMUX0 Register

7.3.5 PINMUX1 Register

Bit	Name	Type	Description
31	EBI_EN	R/W	0x0: Disable EBI IO, 0x1: Enable EBI IO
30-28		R	Reserved
27-26	GPIO29_MUX	R/W	0x0: GPIO29, 0x1: GPI_RST
25-24	GPIO28_MUX	R/W	0x0: SPI0_CSN0, 0x1: GPIO28
23-22	GPIO27_MUX	R/W	0x0: SPI0_CLK, 0x1: GPIO27
21-20	GPIO26_MUX	R/W	0x0: SPI0_MIS0, 0x1: GPIO26
19-18	GPIO25_MUX	R/W	0x0: SPI0_MOSI, 0x1: GPIO25
17-16	GPIO24_MUX	R/W	0x0: UART1_TXD, 0x1: GPIO24
15-14	GPIO23_MUX	R/W	0x0: UART1_RXD, 0x1: GPIO23
13-12	GPIO22_MUX	R/W	0x0: I2C_SDA, 0x1: GPIO22, 0x2: PWM1.1
11-10	GPIO21_MUX	R/W	0x0: I2C_CLK, 0x1: GPIO21, 0x2: PWM1.0
9-8	GPIO20_MUX	R/W	0x0: UART0_RXD, 0x1: GPIO20
7-6	GPIO19_MUX	R/W	0x0: UART0_TXD, 0x1: GPIO19
5-4		R/W	Reserved
3-0		R	Reserved

Table 7-7 PINMUX1 Register

7.3.6 GPIO_PE Register

Bit	Name	Type	Description
31		R	Reserved
30	I2C_SDA/GPIO22/PWM1.1_PE	R/W	Enable I2C_SDA/GPIO22/PWM1.1 pull enable function. 0x0: No pull, 0x1: Pulled HIGH
29	I2C_CLK/GPIO21/PWM1.0_PE	R/W	Enable I2C_CLK/GPIO21/PWM2 pull enable function. 0x0: No pull, 0x1: Pulled HIGH
28	SPI0_CLK/GPIO27_PE	R/W	Enable SPI0_CLK/GPIO27 pull enable function. 0x0: No pull, 0x1: Pulled HIGH
27	SPI0_CSN0/GPIO28_PE	R/W	Enable SPI0_CSN0/GPIO28 pull enable function. 0x0: No pull, 0x1: Pulled HIGH
26	SPI0_MOSI/GPIO25_PE	R/W	Enable SPI0_MOSI/GPIO25 pull enable function. 0x0: No pull, 0x1: Pulled HIGH
25	SPI0_MISO/GPIO26_PE	R/W	Enable SPI0_MISO/GPIO26 pull enable function. 0x0: No pull, 0x1: Pulled HIGH
24	JDAT_PE	R/W	Enable JDAT pull enable function. 0x0: No pull, 0x1: Pulled HIGH
23	JCLK_PE	R/W	Enable JCLK pull enable function. 0x0: No pull, 0x1: Pulled LOW
22	UART1_RXD/GPIO23_PE	R/W	Enable UART1_RXD/GPIO23 pull enable function. 0x0: No pull, 0x1: Pulled LOW
21	UART1_TXD/GPIO24_PE	R/W	Enable UART1_TXD/GPIO24 pull enable function. 0x0: No pull, 0x1: Pulled LOW
20	UART0_RXD/GPIO20_PE	R/W	Enable UART0_RXD/GPIO20 pull enable function. 0x0: No pull, 0x1: Pulled LOW
19	UART0_TXD/GPIO19_PE	R/W	Enable UART0_TXD/GPIO19 pull enable function. 0x0: No pull, 0x1: Pulled LOW
18		R/W	Reserved
17		R	Reserved
16		R	Reserved
15	GPIO15_PE	R/W	Enable GPIO15 pull enable function 0x0: No pull, 0x1: Pulled HIGH
14	GPIO14_PE	R/W	Enable GPIO14 pull enable function. 0x0: No pull, 0x1: Pulled HIGH
13	GPIO13_PE	R/W	Enable GPIO13 pull enable function. 0x0: No pull, 0x1: Pulled HIGH
12	GPIO12/EXT_ INT1/ CLK1_O _PE	R/W	Enable GPIO12/EXT_ INT1/CLK1_O pull enable function. 0x0: No pull, 0x1: Pulled HIGH
11	GPIO11/SPI1_CLK_PE	R/W	Enable GPIO11/SPI1_CLK pull enable function. 0x0: No pull, 0x1: Pulled HIGH

Bit	Name	Type	Description
10	GPIO10/SPI1_CSN/CLK1_O _PE	R/W	Enable GPIO10/SPI1_CSN/CLK1_O pull enable function. 0x0: No pull, 0x1: Pulled HIGH
9	GPIO9/SPI1_MOSI/ EXT_INT0 _PE	R/W	Enable GPIO9/SPI1_MOSI/EXT_INT0 pull enable function. 0x0: No pull, 0x1: Pulled HIGH
8	GPIO8 _PE	R/W	Enable GPIO8 pull enable function. 0x0: No pull, 0x1: Pulled HIGH
7	GPIO7/SPI0_CSN1_PE	R/W	Enable GPIO7/SPI0_CSN1 pull enable function. 0x0: No pull, 0x1: Pulled LOW
6	GPIO6 _PE	R/W	Enable GPIO6 pull enable function. 0x0: No pull, 0x1: Pulled HIGH
5	GPIO5/SPI1_MISO_PE	R/W	Enable GPIO5/SPI1_MISO pull enable function. 0x0: No pull, 0x1: Pulled LOW
4		R	Reserved
3	GPIO3_PE	R/W	Enable GPIO3 pull enable function. 0x0: No pull, 0x1: Pulled HIGH
2	GPIO2/PWM0.1_PE	R/W	Enable GPIO2/PWM0.1 pull enable function. 0x0: No pull, 0x1: Pulled HIGH
1	GPIO1/PWM0.0_PE	R/W	Enable GPIO1/PWM0.0 pull enable function. 0x0: No pull, 0x1: Pulled HIGH
0		R	Reserved

Table 7-8 GPIO_PE Register

7.3.7 AGPIO_CTRL0 Register

Bit	Name	Type	Description
31-28		R/W	Reserved
27	AGPIO_78_AEN	R/W	Select digital or analogue function of AGPIO7 and AGPIO8. 0x0: digital mode, 0x1: analogue mode
26	AGPIO_56_AEN	R/W	Select digital or analogue function of AGPIO5 and AGPIO6. 0x0: digital mode, 0x1: analogue mode
25	AGPIO_34_AEN	R/W	Select digital or analogue function of AGPIO3 and AGPIO4. 0x0: digital mode, 0x1: analogue mode
24	AGPIO_12_AEN	R/W	Select digital or analogue function of AGPIO1 and AGPIO2. 0x0: digital mode 0x1: analogue mode
23	AGPIO8_PE	R/W	0x0: No pull, 0x1: Pulled HIGH
22	AGPIO7_PE	R/W	0x0: No pull, 0x1: Pulled HIGH
21	AGPIO6_PE	R/W	0x0: No pull, 0x1: Pulled HIGH
20	AGPIO5_PE	R/W	0x0: No pull, 0x1: Pulled HIGH
19	AGPIO4_PE	R/W	0x0: No pull, 0x1: Pulled HIGH
18	AGPIO3_PE	R/W	0x0: No pull, 0x1: Pulled HIGH

Bit	Name	Type	Description
17	AGPIO2_PE	R/W	0x0: No pull, 0x1: Pulled HIGH
16	AGPIO1_PE	R/W	0x0: No pull, 0x1: Pulled HIGH
15-14		R/W	Reserved
13-12	AGPIO7_FUNC	R/W	0x2: ACMP_CH[6]
11-10	AGPIO6_FUNC	R/W	0x2: ACMP_CH[5]
9-8	AGPIO5_FUNC	R/W	0x2: ACMP_CH[4], 0x3: SAR_CH[6]
7-6	AGPIO4_FUNC	R/W	0x2: ACMP_CH[3], 0x3: SAR_CH[5]
5-4	AGPIO3_FUNC	R/W	0x2: ACMP_CH[2], 0x3: SAR_CH[3]
3-2	AGPIO2_FUNC	R/W	0x2: ACMP_CH[1], 0x3: SAR_CH[2]
1-0	AGPIO1_FUNC	R/W	0x2: ACMP_CH[7], 0x3: SAR_CH[1]

Table 7-9 AGPIO_CTRL0 Register

8 *Application Information*

8.1 *Sigfox RCZ1,2,3,4,5,6 Reference Circuit*

8.1.1 Uplynx XS8001-T-NG48NRY Power Circuit

The Uplynx XS8001-T-NG48NRY requires voltage to be supplied to pins 6, 46, 47 and 48. The decoupling circuit should be placed close to the SOC as suggested in the layout Gerber file.

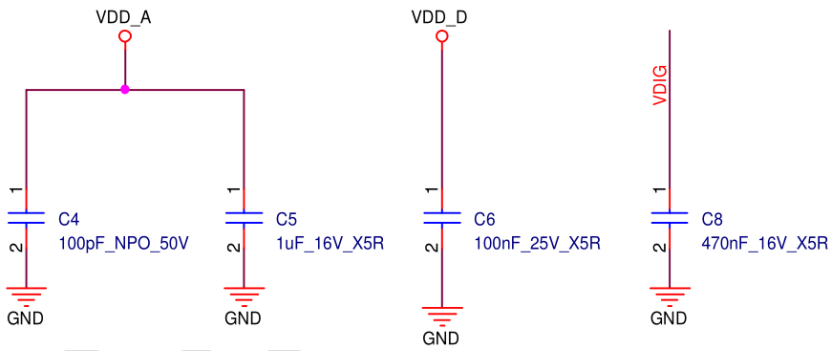


Figure 8-1 Power Decoupling Circuit

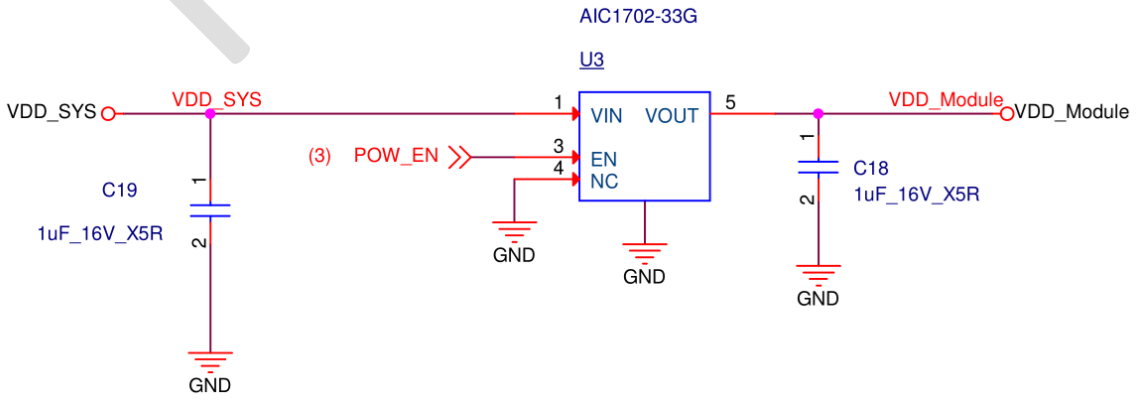


Figure 8-2 LDO Circuit

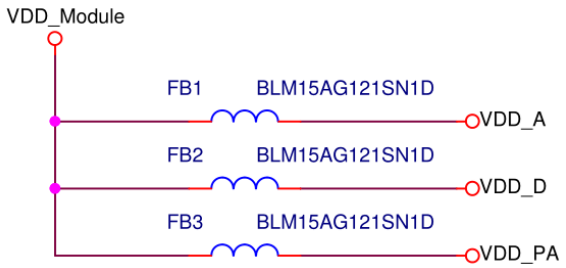


Figure 8-3 Beads between Power Domains

Ferrite beads FB1, FB2 and FB3 are inserted to isolate the power domains VDD_A, VDD_D and VDD_PA respectively from each other and to avoid unwanted noise coupling to the main power supply VDD_module.

8.1.2 Uplynx XS8001-T-NG48NRY clock Circuit

The reference circuit consists of a 24MHz TCXO. A power gating PMOS (Q6) is used to gate off the current drawn when sleep mode is active. On powering on, TCXO_PD is pulled low. The selection of C26 is to ensure proper operating point of XTAL_OUT.

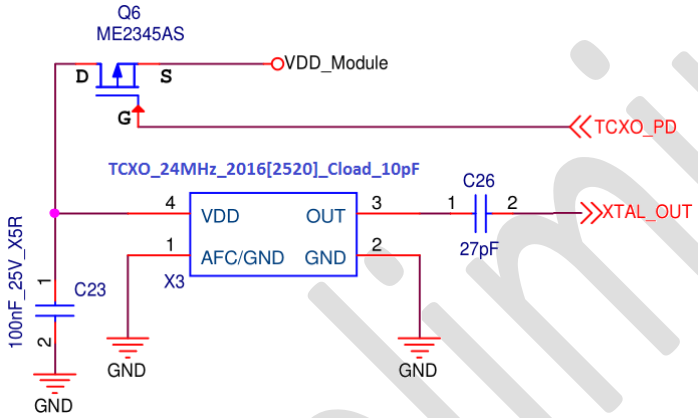


Figure 8-4 24MHz TCXO Circuit

8.1.3 Uplynx XS8001-T-NG48NRY Control Circuit

The Uplynx XS8001-T-NG48NRY is controlled by a dedicated power enabling pin POW_EN. A high level state indicates power ON and low is OFF. When the module is ON, the Sigfox AT command interface is loaded automatically. UART_TX and UART_RX are the pins for the UART interface. AT command is configured for communication through this UART interface at 9600bps (no flow control, 8 data bit, 1 stop bit). The RESET is used to reset the SOC which is active low. A pull up resistor over a capacitor is included in the design as a means of resetting the SOC on startup.

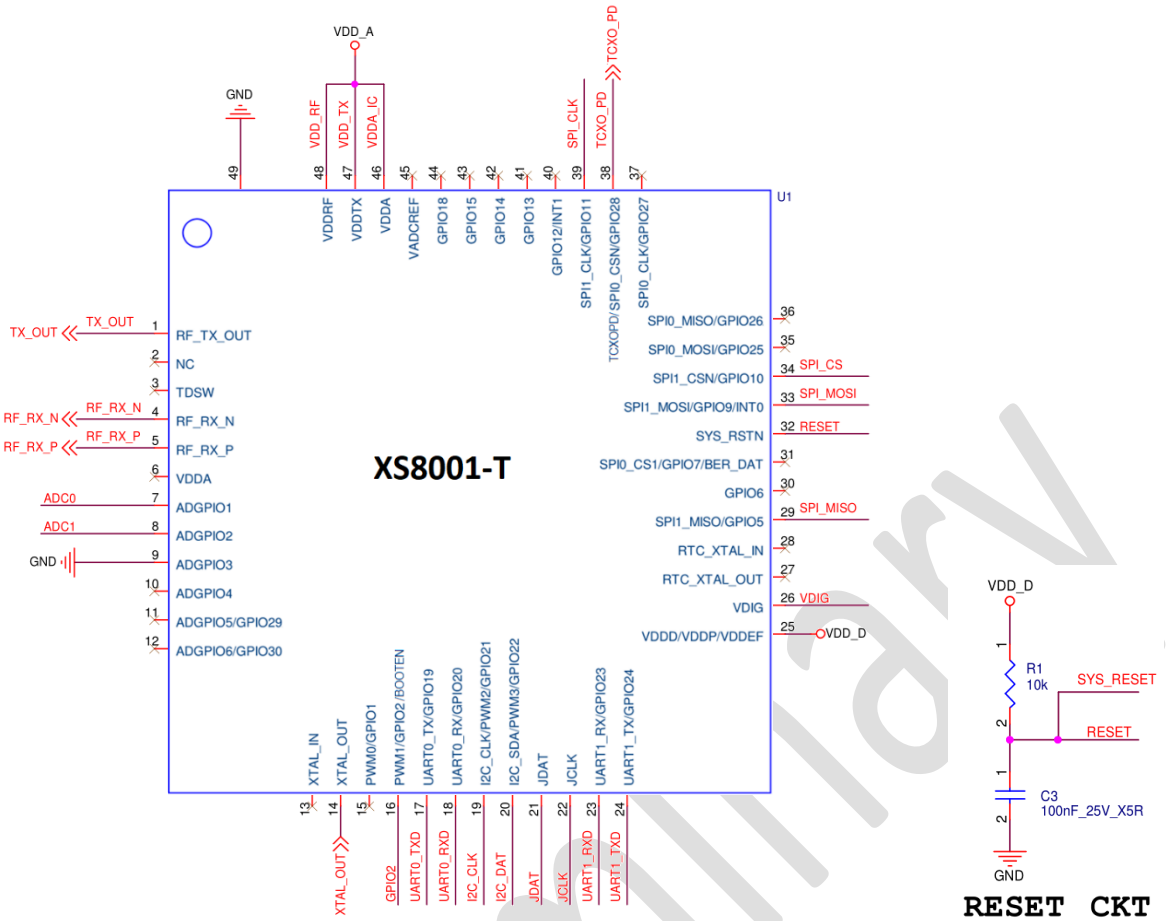


Figure 8-5 Control and Reset Circuit

8.1.4 Uplynx XS8001-T-NG48NRY Radio Frequency Circuit

- *RCZ1,2,3,4, 5 and 6 operation*

  The RF reference circuit consists of the matching and filter circuit for the power amplifier and low noise amplifier which covers the operating frequency of 868MHz, 902MHz to 920MHz which compliant with FCC (FCC-like), CE and ARIB T-108 regulatory requirements[1].

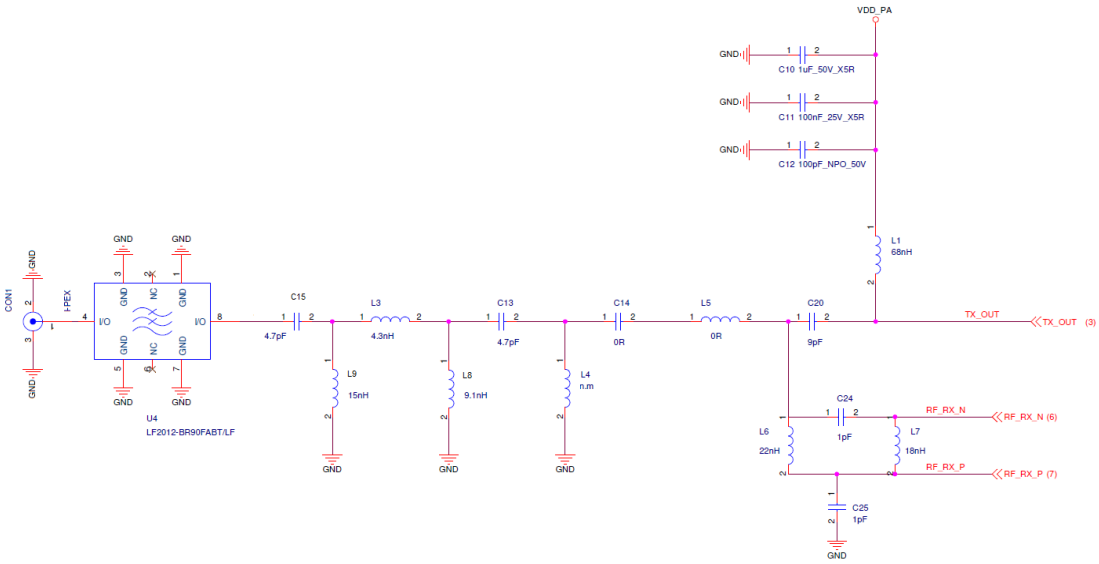


Figure 8-6 RCZ123456 Recommended Sigfox Ref. Design – RF Matching and Filtering Circuit

[1] Test reports can be made available upon request

- *RCZ3 , RCZ4 and RCZ5 operation*

The RF reference circuit consists of the matching and filter circuit for the power amplifier and low noise amplifier. BSM8001-03 module is designed for the region with operating frequency of 902MHz to 920MHz which compliant with ARIB T-108 regulatory requirements[2].

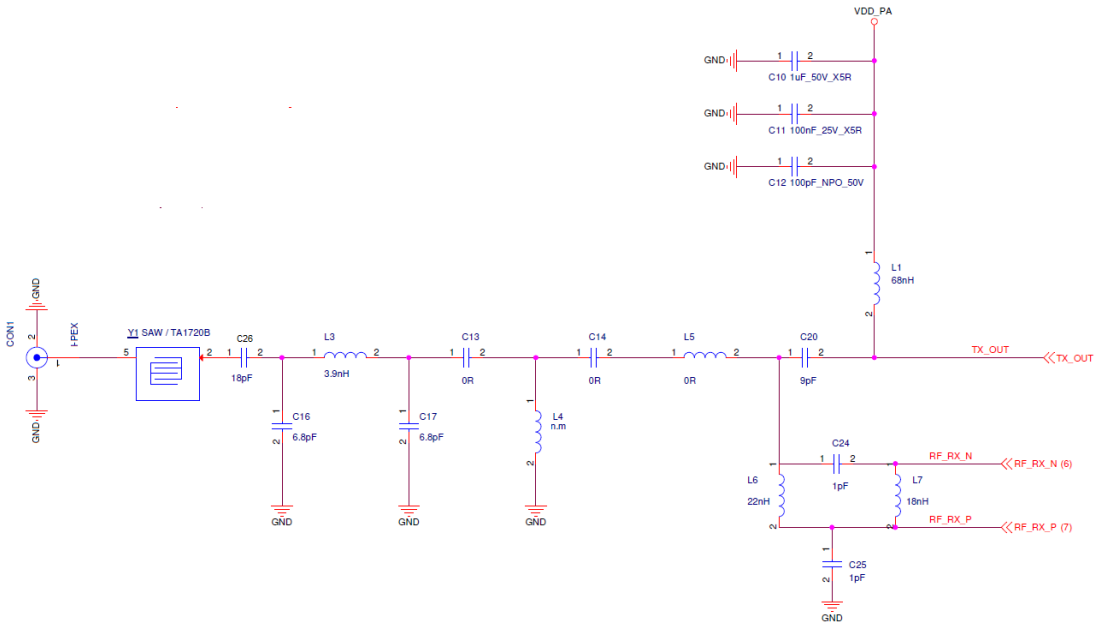


Figure 8-7 RCZ3 and RCZ5 Recommended Sigfox Ref. Design – RF Matching and Filtering Circuit

8.2 *Clock Source Related to Power Mode Support*

The leakage current during sleep can be reduced or completely removed with an external switch or LDO since the Uplynx XS8001-T-NG48NRY is usually a Sigfox modem which an application processor can choose to switch on or off. It is advised to use a 24MHz oscillator or external clock source instead of a crystal if intense sleep and wake up activity is required to ensure short clock settling time.

8.3 *Leakage without VDD on Uplynx XS8001-T-NG48NRY*

When VDD is not supplied to the Uplynx XS8001-T-NG48NRY , user must avoid asserting the digital control signal onto any of the digital interfaces of the SOC; this avoids improper start-up and current leakage.

[2] Test reports can be made available upon request

9 *Design-in options and Production flow*

To design with XS8001-T-NG48NRY for Sigfox product, there are three options

Design-in Option	*Application to Sigfox P1 certification program*	*ID/PAC/AES Key source*	*Preloaded Firmware*	*Suitable for*
Chip on board with application circuit **different** from Sigfox verified reference circuits	**New P1 application is needed**	Directly from **Sigfox** after P1 certification program	*Bootloader only	New product with special requirement on material, form factor
Chip on board with application circuit **identical** to that Sigfox verified reference circuits	**Not necessary** - ESMT Sigfox verified reference design is reused.	**ESMT** provides ID/PAC information and to be programmed during manufacturing process		Low cost system solution or solution targeted at minimal PCBA size
Module on board	**Not necessary** - ESMT Sigfox verified reference design is reused.	**Embedded** in the module	*Bootloader, ID/PAC and Sigfox verified AT command application firmware	All applications

* Sigfox Verified AT command application firmware & firmware built based on ESMT SDK can be uploaded via Bootloader command

9.1 *Chip on Board manufacturing flow*

An application note "Uplynx Products (Addendum – Project Development and Production Test" described the procedure in details. Basically, the DUT needs to be tested for RF compliance, RF output power and the frequency offset and temperature sensor calibrated words are to be written into the flash area in the DUT at the end of the manufacturing test procedure.
The complete production flow with XS8001-T-NG48NRY have been developed in LitePoint IQFlex and one may contact Sales and representatives of LitePoint.

9.2 *Module on Board*

Every module is tested thoroughly before shipment, simple RF packet power and frequency offset test would be enough to ensure proper operation.

10 *Appendix:*

10.1 *PCB Guidelines*

PCB Stack Up

Layer	Material	Thickness	Dielectric
	Soldermask	0.7 mil	
L1	Cu + Plating	1.4 mil	
	Prepreg	4.3 mil	3.7
L2	Cu	1.2 mil	
	Core	24.0 mil	4.4
L3	Cu	1.2 mil	
	Prepreg	4.3 mil	3.7
L4	Cu + Plating	1.4 mil	
	Soldermask	0.7 mil	
	Total thickness	39.2 mil	
		1.0 mm	
Material: FR4 - 50Ω / W:27 mil / D:7.5 mil TOP Layer			

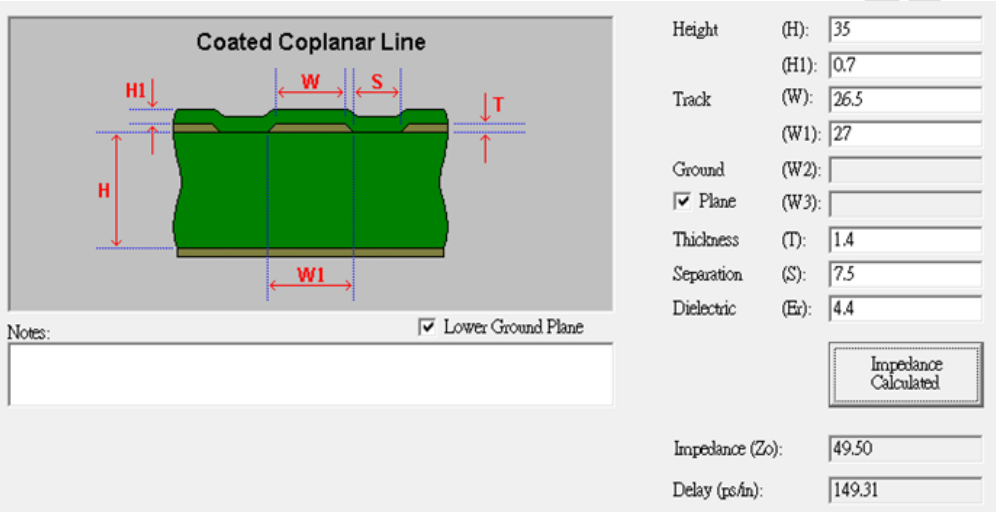


Figure 10-1 PCB stacking

Layout Guide

- The choke inductor (L1) must be placed as close to the RF_TX_OUT pin of the Uplynx SOC as possible.
- All the bias bypass capacitors should be kept as close to the bias pins as possible.
- The exposed pads of the Uplynx SOC should be connected to the ground layer below with the maximum number of vias possible. The exposed pads should also be connected to the top layer ground metal to further improve RF grounding using diagonal trace connections where possible.
- The crystal should be placed as close as possible to the Uplynx SOC. The crystal capacitors should also be placed near to the crystal pads.
- A four-layer board is strongly recommended. Put the ground layer very close to the top layer to obtain a good ground plane reference. A thickness of 0.2mm or 0.3mm between the top layer and ground layer is suggested.

- Connect all the ground metallization and/or layers with as many vias as possible. It is also recommended that the ground return path between the ground vias of the TX and RX networks and the ground vias of the Uplynx SOC not be blocked in any way: the return current should see a clear unhindered pathway through the ground plane to the back of the Uplynx SOC.

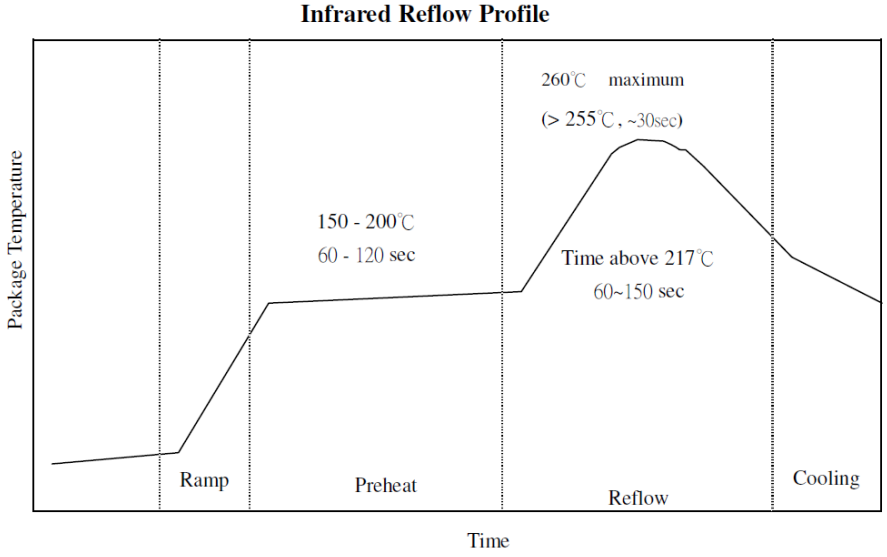
10.2 *MSL Ratings*

The MSL rating of an IC determines its floor life before the board mounting once its dry bag has been opened. IPC/JEDEC J-STD-033C is the electronics industry standard for defining MSL ratings versus floor life at 30°C, as shown in Table 1.Reflow Profile

XS8001-NG48NRY and XS8001-T-NG48NRY are rated MSL3.

10.3 *Recommended Soldering Condition for Lead-Free application*

The temperature of package top surface shall be monitored at the same time, to validate that the peak package body temperature (TP) does not exceed the MSL classification of individual devices (see IPC/JEDEC J-STD020).



Note:

- The IR reflow profile is referencing to IPC/JEDEC J-STD-020D.
- Time above 150℃ should be minimized not to damage PCB material.
- The maximum package body temperature should be limited to 260℃.
- The re-flow should not be repeated for more than two times.(≦2 times re-flow is acceptable)
- Temperature ramp-up rate: 0℃/sec to 3℃/second. Ramp-down rate : 0℃/sec ~ 6℃/sec.
- Actual heating: Temperature 260℃ Max., 255℃or more for 30 sec.
- Actual re-flow time is influenced by component density and package dimension on board.
- The above condition is only for some particular package molding compounds (targeted for lead-free application).

11 *Order Information.*

Product Name	Order Part Number	Description
XS8001-T-NG48NRY Sigfox System on Chip	XS8001-T-NG48NRY	High performance Wireless MCU with Sigfox uplink